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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
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International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/NO01/00113	15/03/2001	15/03/2000
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Applicant THIN FILM ELECTRONICS ASA		

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1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 4 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of ~~24~~ 21 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
16/10/2001	19.06.2002
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Kusztelan, L Telephone No. +49 89 2399 2479

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/NO01/00113

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:
Description, pages:

1-~~21~~ 18	as received on	23/05/2002	with letter of	16/05/2002

Claims, No.:

1-14	as received on	23/05/2002	with letter of	16/05/2002

Drawings, sheets:

1/16-16/16	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   - ☐ the description, pages:
   - ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-14
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-14
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-14
	No:	Claims	

2. Citations and explanations
   see separate sheet

Section V

The document D2 is regarded as being the closest prior art to the subject-matter of claims 1,10. The subject-matter of claims 1,4 differs in that electrical edge connections lying over the layer edges & deposited on their surface are provided to contact contact pads. The subject-matter of claims 1,10 is therefore novel. An inventive step is appreciated in that the cited documents do not lead the skilled person to consider such a method of connecting stacked & staggered layers.

Vertical electrical interconnections in a stack

The present invention concerns a memory and/or data processing device having at least two stacked layers provided in a stack, wherein the stack either forms a self-supporting structure or alternatively is provided on a substrate, and wherein the stack comprises at least one structure staggered in at least one direction, such that steps in the staggered structure are formed by exposed portions of the separate layers in the stack and with a step height h corresponding to the thickness of the respective layers. It also concerns a method for fabrication of a memory and/or data processing device which comprises at least two layers provided in a stack, wherein the stack either forms a self-supporting structure or alternatively is provided on a substrate, and wherein the stack comprises at least one structure staggered in one direction, such that steps in the staggered structure are formed of exposed portions of the separate layers in the stack and with a step height h corresponding to thickness of the respective layers.

Modern electronic microcircuits are typically built layer by layer on silicon chips in a series of process steps where insulating layers separate layers containing metallic, insulating and semiconducting materials that are patterned and processed by various deposition and etching techniques. Integral to the ensuing architectures are electrical connections between components and sub-circuits which are located in the substrate and in layers on top of the substrate. These connections, termed vias, are typically in the form of metallic posts or wires that penetrate through one or more layers of intervening material separating the components to be connected. Such vias are either made during the layer-building process or they are inserted through already existing layers by creating channels through the layers (by e.g. etching), followed by filling metal plugs into the channels.

Silicon chips according to prior art may involve 20-30 masking steps, and the number of separate layers containing patterned metal intra-layer leads that connect directly or indirectly to a via is typically 3-5. Each via requires a certain amount of real estate associated with it in each layer that is traversed or connected. In addition to the metal cross section of the via itself, there must be allocated a buffer zone around it which insulates the via from adjacent circuitry that shall not be in immediate contact with the via, and

allowance must be made for the finite precision with which the patterning in each layer can be made as well as registration accuracy of patterning masks.

In the paper "A review of 3-D Packaging Technology" by S.F. Al-sarawi, D. Abbott and P.D. Franzon, IEEE Transactions on components, packaging, and manufacturing technology, part B, volume 21, No. 1 (Feb. 1998), there is given a survey of the state of the art with regard to three-dimensional packaging technology aimed at large scale integration. Herein there is in several places referred to how whole stacks of integrated circuit chips can be connected mutually electrically, among other with the use of vertical vias and current paths provided on the side surfaces of circuit chip stacks, as well as the use of bonding wires for connecting respectively the mother and daughter chip where the daughter chip is provided stacked upon the mother chip, such that the exposed surface of the mother chip form a step of the stack. In this case bonding wires which are mechanically connected to contact points on the chips are used.

Wholly generally there is besides in Norwegian patent No. 308 149 and in Norwegian patent application No. 19995975 disclosed memory and data processing devices where the separate layers in the stack substantially are made with sublayers of thin film in organic material and wherein conductors at the thin films in the separate layers are conveyed to electrical edge connections on the side of the layers. In Norwegian patent application No. 19995975 the connection between the layers may additionally also be formed by vias which in principle will be fabricated as conducting structures in the same material which is included in the thin film and hence form an integral part thereof, and there is further shown a concept called "staggered vias" wherein the separate layers in a stack of this kind are provided mutually staggered and the layers in the stack connected mutually electrically or to an underlying substrate by the use of so-called staggered vias over the staggered portion. Neither in Norwegian patent 308 149 nor in Norwegian patent application No. 19995975 there are given any directions how the disclosed edge connections can be realized in a physical and practical embodiment.

The above referred prior art has generally proved in adequate for devices built on silicon substrates as mentioned above, where the number of layers and vias is low to moderate, and where ultra-high precision lithography is an integral part of the chip-making process. However, vias represent a considerable complicating feature in the overall manufacturing process, with consequences for yield and costs. Furthermore, it is expected that entirely new types of device architectures and manufacturing methods for electronic

data processing and storage devices shall emerge in the next few years as serious contenders for large commercial segments. A common feature of such new architectures shall be that they incorporate thin-film electronics in dense stacks containing very large numbers of layers. In many instances, these devices will be manufactured by high-volume technologies such as reel-to-reel processing on thin polymer substrates. In this context, traditional via connection technologies shall be totally inadequate, technically as well as cost-wise.

It is a major object of the present invention to provide methods and technical solutions whereby electrical interconnects can be created between layers and/or between layers and an underlying substrate, in memory and/or processing devices that incorporate a stack containing two or more sheet- or film-like functional parts that partially or completely overlap each other.

It is also an object of the present invention to provide such methods and technical solutions that can be implemented in cases where the number of such sheet- or film-like functional parts becomes large, typically exceeding 5-10.

It is a further object of the present invention to provide such methods and technical solutions that can be implemented in cases where such sheet- or film-like functional parts are manufactured and devices assembled by high-volume, low-cost technologies.

The above-mentioned objects and further features and advantages are realized according to the present invention with a device which is characterized in that one or more contact pads are provided on each step in the staggered structure in electrical connection with memory and/or processing circuits in the respective layer, and that one or more electrical edge connections are provided on and over the step in each layer in the form of electrical conducting structures on the step and over the edge between the steps in each layer and deposited on the surface of the layers, the electrical edge connections contacting one or more contact pads in the layers and providing electrical connection between each layer and also between the layers and contact pads provided on an optional substrate.

In the device according to the invention it is considered advantageous that two or more contact pads (4) in one or more layers (L) are mutually

connected by electrical conducting structures provided on the step in the respective layer. Further there is in the device according to the invention regarded as advantageous that the electrical edge connections are provided as continuous current paths between contact pads in at least three consecutive layers in the stack or between contact pads in at least two adjacent layers in at least two adjacent layers in the stack and an optional substrate adjacent to one of these layers and/or that the electrical edge connections are provided as a patched current path between two adjacent layers in the stack or between an optional substrate and the layer adjacent to the substrate.

Preferably the stack in the device according to the invention forms at least a part of a step pyramid structure, such that the layers have different areas.

In an advantageous embodiment of the device according to the invention the separate layers in the stack are mutually displaced, such that the staggered structure comprises at least one staggered portion where the steps form an exposed portion of an upper surface in the respective layers in the stack and at least one staggered portion where the steps form an exposed portion of a lower surface in the respective layers in the stack, one or more contact pads on each step in each case being electrically connected with conducting structures respectively provided on opposite surfaces of the layers.

In another advantageous embodiment of the device according to the invention, wherein the stack is provided on a substrate, the stack forms at least a part of an inverted step pyramid-like structure, such that the area of each layer increases with the distance from the substrate, and that overlying layers are carried over the edges of underlying layers and to rest against the substrate, overlying layers being formed with one or more staggered portions, whereby the number of steps in the staggered portion of a layer corresponds to the number of layers located therebeneath, and preferably are then one or more contact pads provided in the substrate where the layers are resting against the substrate.

Finally there is in the device according to the invention regarded as advantageous that the side edge of each layer between the steps is rounded or forms an inclined surface.

The above-mentioned objects and further features and advantages are also realized according to the invention with a method which is characterized by

adding each layer in the stack in separate succeeding steps, providing each succeeding layer in the stack with an area different relative to the previous adjacent layer or displaced in relation thereto, such that the stack is formed with the at least one staggered structure in one direction, steps in the staggered structure being formed by exposed portions in the provided layers, depositing structures of conducting material on the steps in each layer, such that one or more current paths and one or more contact pads are formed on each layer, and depositing continuous and/or patched electrical conducting structures which form electrical edge connections between the contact pads on two or more layers and/or between the contact pads or one or more layers and the substrate.

In the method according to the invention it is regarded as advantageous depositing depositing the layers such that the stack forms at least a part of a step pyramid structure, or depositing the layers such that the stack forms at least a part of an inverted step pyramid structure, each overlying layer being deposited over the edge of an underlying layer and to rest against the substrate, whereby overlying layers are formed with one or more staggered portions, the number of steps in each staggered portion in a layer corresponding to the number of layers located therebeneath.

In the last-mentioned case one or more contact pads are preferably provided in the substrate where the layers rest against the substrate.

Finally there is in the method according to the present invention regarded as advantageous forming the electrical edge connections in a process selected among one of the following, viz. lithography, dry etching, ink jet printing, silk printing, soft lithography, electrolysis, electrostatic deposition or in situ conversion.

In the following the invention will be described in greater detail with a discussion of exemplary embodiments and with reference to the accompanying drawing figures, of which

fig. 1a shows a side view of a first generic device according of the present invention,
fig. 1b a plan view of a first embodiment of the device in fig. 1a.
fig. 1c a plan view of a second embodiment of the device in fig. 1a,
fig. 2 a plan view of a third embodiment of the device in fig. 1a,

fig. 3 a plan view of a fourth embodiment of the device in fig. 1a,
fig. 4a-c analog embodiments of the device in fig. 1a without use of substrate,
fig. 4d a side view of a variant of the embodiments in fig. 4a, but with possibility of accessing from both sides,
fig. 5a-e a first example of fabrication steps for forming a device of the kind shown in fig. 1a,
fig. 6a-d a second example of fabrication steps for forming a device of the kind shown in fig. 1a,
fig. 7 a side view of a second generic device according to the present invention,
fig. 8a-e an example of fabrication steps for forming a device of the kind shown in fig. 7,
fig. 9a geometric relationships in the patterning of electrical edge connection on to the device in fig. 1a,
fig. 9b geometric relationships in the patterning of electrical edge connections on the device in fig. 7,
fig. 10 schematically the layout of the electrodes in a passive matrix-addressable device according to prior art, and
fig. 11a-m examples of fabrication steps for forming a stacked matrix-addressable memory device based on the device according to the present invention.

Before a closer description and discussion of examples of embodiments of the device according to the present invention are given, a short exposition of the general background of the invention will be presented.

As thin-film based active circuitry employing inorganics, oligomers or polymers enters the mainstream of commercial electronics, it is expected that stacked devices with "smart" layers, i.e. layers that possess individual processing capabilities, shall become ubiquitous. In addition to enhancing the possibilities inherent in the stacking concept, this implies that bus-type edge connections may carry messages that are distributed globally across the stack and picked up selectively by those layers they are intended for. On the other hand, the interconnect concepts of the present invention may involve stacks that contain sheets or layers without decoding circuitry, in which case dedicated edge connections to those sheets may have to be provided. An extreme case of the latter is where all layers are "dumb" and where each

layer has dedicated electrical connections to driving circuitry on a supporting substrate or circuitry at a cable-connected location elsewhere. In what follows, these different aspects of possible electronic capabilities in individual layers shall not be treated in any further detail, since the appropriate choices of solutions according to the present invention will be obvious to a person skilled in the art.

Now a more specific description of generic devices according to the present invention, examples of embodiments thereof as well as a exposition of fabrication steps in preferred embodiments of the method according to the invention shall be given, such that these can be used for realizing embodiments of the device according to the invention.

Specifically fig. 1a shows a side view of a first generic device according to the invention. This generic device can be denoted as a step pyramid structure. It comprises stacked functional units which are provided on separate, but mutually adjacent sheet-like or film-like layers provided on a substrate. Circuits on the top surface of a given layer are electrically connected with contact pads on an exposed edge area of the layer. In the side view in fig. 1 there are shown four such layers L_1-L_4 which together forms a stack 1. As shown in the side view the layers L_1-L_4 on the right side form a staggered structure and above this an electrical edge connection 3 is provided and extends from the top surface of the layer L_4 and down to a contact pad 5 on the substrate 2. The electrical edge connection 3 contacts and is connected with electrical conductors provided on the top surface of each layer L and indicated by a thicker, not specifically denoted line, such this is apparent from fig. 1a.

Fig. 1b shows a first embodiment of the device in fig. 1a and it will here be seen that the layers L_1-L_4 in the stack 1 is staggered in one direction, namely towards the right. On each of the layers L_1-L_4 there are then provided contact pads 4, one of which is emphasized in the figure, and an electrical edge connection 3 is now provided such that it contacts the contact pads 4 and then connects the layers L_1-L_4 electrically to contact pads 5 on the substrate 2. The contact pads in the layers L_1-L_3 are provided in an exposed portion thereof which form the steps in the staggered structure. In fig. 1b there is in the top layer shown a rectangular hatched area which represent a circuit area. Without this being shown in detail, the circuit area can consist of physically

separate components and networks or circuits connected in one or more networks, and in case of the embodiments in fig. 1b, two connecting paths 3 to the substrate are shown. It is of course to be understood that both in fig. 1b and the additional figures theis hatched area in the top layer will have its equivalent in corresponding circuit areas in the other underlying layers.

In fig. 1c there is shown a plan view of another embodiment of the device in fig. 1e where the stack 1 with the layers L_1-L_4 now is staggered in two mutually orthogonal directions, providing a much greater exposed step area which can be used for connecting purposes. This embodiment also allows alternative and more dispersed locations of the contact pads 4, the exposed portions as well as the contact pads 5 on the substrate. Simultaneously there is achieved good separation between the two edge connections 3 which contact the contact pads 4 in all layers and additionally the contact pads 5 on the substrate, as the edge connections are provided in each of the two stagger directions.

Fig. 2 shows a fourth embodiment of the device in fig. 1a, but as will be seen, the edges to the separate layers L_1-L_4 in the stack 1 are here rounded in the step area and this may offer advantages when the edge connection which here is denoted 6, shall be carried over the steps formed by all layers and down to the substrate 2. If the step is not perpendicular, but rounded, the embodiment in fig. 2 shall reduce the risk for a rupture in the electrical edge connection. When it is carried over a sharp edge, such as is the case in the embodiments in figs. 1a-c, there will always be a certain danger for a rupture arising in an edge connection formed as a deposited thin conducting layer. In a variant of the embodiment in fig. 2 the steps need not be rounded, but can be formed with a gradual slope between the separate steps.

Fig. 3 shows a fourth embodiment of the device in fig. 1a and wholly in analogy with the embodiment in fig. 1c. Also here the stack 1 comprises four layers L_1-L_4 provided on a substrate 2 which correspondingly to the embodiment in fig. 1c are provided with two contact pads 5. However, only one of the edge connections 3 is provided as a continuous connection from the uppermost layer L_4 and to the contact pad 5 on the substrate and simultaneously contacting all contact pads 4 on the exposed portions, i.e. the steps in the layers L_1-L_4 as shown. There are also provided several contact pads 4 on each of the steps in the layers as shown at the lower right in the

stacked structure 1. Here it is e.g. provided three contact pads 4 on each step and this offers possibilities for independent connections between two or more layers mutually over a short edge connection 3 as shown and additionally possibilities for patching of electrical connections both between separate layers and mutually within a layer as shown for the layer L_1, possibly with additional further edge connection 3 to the contact pad 5 on the substrate 2.

It is to be understood that according to the present invention it will also be possible to form the stack 1 as a polygonal pyramid with 3,4,5 etc. stagger directions, but it will be obvious to persons skilled in the art that this is only a direct extension of the principle of the embodiments as exhibited in figs. 1b and 1c and hence they shall not be more closely described here.

Figs. 4a-c show embodiments of the first generic device according to the present invention with the electrical edge connections 3 schematically indicated as lines between and above the layers. It is distinguished above the one in fig. 1a in that stack 1 is not provided on a substrate, but that the layers L are self-supporting structures. Fig. 4a hence shows in side view an analog embodiment to that in fig. 1a, but without substrate. The stack 1 comprises 5 self-supporting layers L_1-L_5 and there is on every step in the stack provided contact pads 4 and for each of the layers L_1-L_4 an edge connection 3 connected with the contact pads 4. Fig. 4b shows a self-supporting device embodied as either a regular step pyramid or alternatively as a polygonal step pyramid. At right the edge connection 3 via the contact pads 4 on the layers L_1-L_4 forms a continuous connection between all layers from L_1 to L_5 with the use of several current paths as well as patching as indicated in fig. 4b at the left where it will be seen that contact pads 4 only are provided on the exposed portions of L_2 and L_3. In this manner it is easy to form an electrical connection between two or more of the layers in the stack 1 and these need not be adjacent. Correspondingly fig. 4c again shows the stack 1 as a step pyramid structure, but with edge connection 3 in at least two stagger directions. In fig. 4 the edge connection here is provided diametrically opposite on each side and contact pads 4 are provided on each step of the structure as here shown with 6 layers L_1-L_6.

The first generic device according to the invention can in addition particularly be realized with the possibility for two-sided contacting, as this is shown in fig. 4d. In order to form separated step areas which expose both

surfaces of each of the five layers L_1-L_5, these which very well may have the same extension, are stepwise mutually staggered. Hence both surfaces of each layer L with edge connections 3 and contact pads 4 on each of the steps, i.e. the exposed portions of the layers are contacting, as these portions on one side of the step form an inverted step structure in relation to the corresponding portions of the opposite side and hence admit access to the opposite surface of each layer L. Beyond that, the layout of the edge connections 3 and the contact pads 4 are the same on both sides of the device as shown in fig. 4d.

Generally the edge connections 3 in the embodiments shown in figs. 1-4 could be formed in each separate layer by using the edge areas specifically for contact purposes, the edge area being formed in an exposed portion of each layer in the stack 1 and these exposed portions being formed by realizing the stack as a staggered structure with staggering in one or more directions, as mentioned above. The steps will, of course, be exposed when the contacts are made.

Generally each layer L in the stack 1 itself can also be formed as a sandwich of the sublayers which may comprise electrical conductors, active circuits and functional materials, e.g. memory materials for data storage purposes. When each layer is built as a sandwich of such sublayers, preferably in thin-film technology, separate sublayers can be realized with specific functional purposes, e.g. in order to achieve contacting and conducting functions or they may comprise active circuits, e.g. formed in thin-film technology or wholly consisting of functional materials, e.g. memory materials for data storage purposes. Without entering into details, it will be evident for persons skilled in the art that each separate layer can be fabricated on a supporting film before it is mounted in the stack or it can be formed by a deposition process or a series of such on a surface of the stack itself. In each case must each sublayer then have a thickness, the lower limit of which will be given by the carrying capacity of the supporting layer in relation to the forces it is exposed to during the prefabrication and stack addition processes. By using additive processes the thickness of single layers can be made much smaller, as the sublayers basically could be deposited as monolayers.

There shall now be given a more detailed description of how the edge connections expediently can be realized in the device according to the invention. In the embodiments as specifically shown in figs. 1-3 the edge connection can be formed by a single electrode deposition or a sequence of deposition operations, such this shall be mentioned in more detail below. In the latter case each deposition operation implies that only a smaller part of the total edge height shall be negotiated, i.e. a single step in the edge structure, and the continuity of the edge connection over a plurality of steps will then be obtained by the sequentially deposited electrodes overlapping.

Techniques for forming edge connections with high precision include lithographic methods based on wet etching or dry etching as well as particle milling, high precision stamping such as soft lithography, and electrolysis. Common to most of these techniques which provide high solution is limited depth of field which in its turn limits the height of each separate step or the number of steps which can be connected electrically in a single production step. In such cases a simple application of a common conductor which e.g. forms a power supply line, bus line etc. can be employed.

Figs. 5a-e show a first example of fabrication steps for generating edge connections in the stack which forms the device according to the invention. Specifically fig. 5a shows the substrate 2 before the deposition of the layers L which form the stack 1 itself. A circuit area C_S is provided in or on the substrate 2 and can in itself form a circuit and this circuit area is further connected with contact pads 5 of the substrate. In the next fabrication step shown in fig. 5b an isolation layer I_{L1} is provided and the denomination thereof shows that it is connected with the first layer L_1 in the stack. For the isolation layer I_{L1} now a circuit C_{L1} is provided for the layer L_1 and connected with contact pads 4 provided on the isolation layer I_{L1}. Fig. 5c renders the same fabrication step for the layer L_2, here with an isolation layer I_{L2} which is provided and laid out such that the resulting layers L_1 and L_2 now shall form a staggered structure. Also on the isolation layer I_{L2} there is provided a circuit area C_{L2} and contact pads 4 connected with this circuit area. Fig. 5d then shows the deposition of a third isolation layer I_{L3} for the third layer L_3 in the stack and with a corresponding circuit area C_{L3} and contact pads 4 connected therewith. The example shown in figs. 5a-5d illustrate how layers L_1-L_3 are formed consisting of respective isolation layers I_{L1}-I_{L3} and circuit areas C_{L1}-C_{L3} connected with respective contact pads

4. In a final fabrication step continuous current paths or conductive paths 3 are provided and form the edge connections which now connect all contact pads 4 mutually in each of the layers and with the contact pads 5 on the substrate.

Instead of depositing the edge connections 3 in one single operation, they can as mentioned also be deposited stepwise such this shall be discussed with reference to fig. 6, which in regard of the separate layers and sublayers shows these formed correspondingly to those in fig. 5, but otherwise illustrates stepwise deposition of the edge connections 3.

Fig. 6a shows a substrate 2 with a circuit area C_S and contact pads 5, while fig. 6b shows a substrate 2 with a provided isolation layer I_{L1} and circuit area C_{L1} for a first layer L_1 in the stack. There are now deposited edge connections 3 over the edge on the isolation layer I_{L1}, these edge connections creating contact between the circuit area C_{L1} and the contact pads 5 on the substrate 2. In fig. 6c another isolating layer I_{L2} is deposited with a circuit area C_{L2} as well as edge connections 3 which are carried over the edge of the isolation layer I_{L2} and down to the edge connection 3 on the underlying isolation layer I_{L1} such that contact pads 4 are formed on the edge connections 3 deposited in fig. 6b. The process is repeated in fig. 6d for a third layer L_3 with isolation layer I_{L3}, circuit area C_{L3} and further edge connections 3 with contact pads 4. This results in that the embodiment as shown in fig. 6d realizes a contiguous, but stepwise deposited edge connection 3 from the uppermost layer in the stack and over contact pads 4 in the interlaying layers and down to the contact pads 5 in the substrate. This also implies that the deposition and contacting operation for each edge connection 3 in itself is handled stepwise and repeatedly and hence any desired height of the stack can be negotiated. The field of depth which is obtained with deposition processes based on photolithographic technique hence only needs to be adapted to an actual step height and in principle the height of the separate step can then precisely correspond to the actual and limited depth of field which is obtained with high resolution photolithography for fabrication of edge connections 3.

In fig. 7 there is shown another generic device according to the present invention. This one is also embodied as a kind of step pyramid, but turned upside down and could hence be called an inverted step pyramid. Similar to

the device in fig. 1 the device in fig. 7 also consists of layers L_1-L_4 which form a stack 1 of functional units in the device. The stack 1 with the layers L provided on the substrate 2 and the concept "inverted step pyramid" is based on the fact that it is the first layer L_1 in the stack 1 which has the smallest area, but the area of each layer increases with the distance from the substrate. A layer which is overlying another is extending beyond this and above the edge of the underlying layers, such each separate layer L in the stack 1 obtains a portion resting directly against the substrate 2. For each of the layers L there are on the substrate provided one or more contact pads 5 such this is shown in fig. 7, and these contact in each of the layers L edge connections 3 which connect circuit areas of functional units in these layers with the substrate. The edge connections 3 are carried over the edges of the steps formed in the separate layers L and down to the substrate 2. In the device in fig. 7 it is achieved that e.g. the separate layers have direct electrical connection to e.g. driver and control circuits provided in the substrate 2, such this can be case if the substrate is formed of a silicon chip.

Now an example shall be given on how a stack 1 which forms an inverted step pyramid as shown in fig. 7 can be fabricated. In fig. 8a a substrate 2 is shown with contact pads 5. A first isolation layer I_{L1} is provided over a substrate 2 such this is shown in fig. 8b and provided as herein shown with two electrodes E_{L1} which via the edge connections 3 are connected with contact pads 5 on the substrate 2 such as rendered in fig. 8c. It is to be understood that there on the isolating layers I_l can be formed circuit areas and not in detail shown functional units which via the electrodes E_{L1} are contacted to an underlying layer. Fig. 8d now shows how the next layer is formed by providing an isolation layer I_{L2} over the first isolating layer I_{L1}, but extending beyond the latter and forming a step over the edge and down to the substrate where a portion of the layer I_{L2} at least extends all the way to contact pads 5 on the substrate. Again electrodes E_{L2} as shown in fig. 8 are provided for connecting circuit areas and functional units in the second layer with the substrate via contact over an edge connection 3 and down to the contact pads 5 in the substrate. Fig. 8f shows how the process is repeated with deposition of yet another isolating layer I_{L3} which masks the electrodes E_{L2} and as shown in fig. 8g is provided with an electrode set E_{L3} which contacts the contact pads 5 on the substrate 2. Hence a stack as shown in figs. 8a-g is obtained with three stacked layers, but which in contrast to the device in fig. 1a is provided as an inverted step pyramid, i.e. the area of each layer

increases with its distance in the stack from the substrate 2. It will be seen that the device in fig. 7 realized as shown in figs. 8a-8g provides separate access between the substrate 2 and the overlying layer L in the stacked structure 1. In this manner the method as illustrated by figs. 8a-8g contrasts with the methods as shown in figs. 5 and 6.

By using photolithographic technique for patterning electrodes, current paths, edge connections etc. in a stack, a relatively small depth of field may entail that there at most can be patterned a few steps at a time and if the number of layers in the stack is large, this implies that a photolithographic operation must be repeated a number of times, something which makes the fabrication of the device both more complicated and additionally increases the cost in no small degree. In order to avoid that the number of operations increases with the number of stacked layers and the number of steps in the stack, an alternative method for photolithographic patterning of contacts and current paths can be used such that the outcome is only one single operation for each layer, while all steps in the stack can be negotiated. This is shown in fig. 9a for the device on fig. 1a. Here the stack 1 which is not shown provided on a substrate, is staggered on the side such that the slope becomes linear. The necessary depth of field hence will be less and approximately equal to the largest height h_{MAX} of one of the layers L in the stack 1. Neither is it necessary that all layers in the stack has the same step height, cf. that in fig. 9a the layer L_2 has a much smaller height than the other layers. The required depth of field as shown by the distance between the parallel stitched sloping lines to the right extends over the whole height of the stack. Optimally the ray direction can be orthogonal to the slope line of the steps. A corresponding situation such it will be for the device shown in fig. 7 is shown in fig. 9b and it will again be seen that the necessary depth of field will be less or equal to h, where h is the height of one of the steps L_1-L_4 in stack, which here is located on a substrate provided with contact pads 5. Again the edge connections can be patterned from top to bottom in one single photolitographic operation, e.g. by letting the ray direction be orthogonal on the slope line as shown by the stitched lines in the figures.

Each separate layer L in the device in fig. 1a or in fig. 7 can be realized as a passive matrix-addressable device such as shown in fig. 10. It comprises a first set of electrodes E_W comprising mutually parallel stripe electrodes W and another set of electrodes E_B which likewise comprises mutually stripe

electrodes B, but provided orthogonally to the electrodes W in the electrode set E_n. A functional material, e.g. a memory medium or a light-emitting medium, can now be provided in sandwich with respectively the electrode set E_B and E_W. An architecture as shown in fig. 10 can be used for realizing a passive matrix-addressable ferroelectric memory device, where the memory medium then in case of a ferroelectric memory material, e.g. an inorganic or organic material, and in the latter case especially preferred a polymer or copolymer. The separate memory cells in a memory of this kind will be formed in the crossing point between the electrodes W which realizes word lines and electrodes B which realizes bit lines in the memory device. If the electrode arrangement is used in a display where the electrodes in at least one set of electrodes will be realized in transparent material, correspondingly the pixels could be formed in the light-emitting material provided in sandwich between the electrode sets E_W,E_B and in the crossing points between the electrodes in the respective sets. In a memory device of the kind mentioned a given memory cell can be written, read and erased by activating the word line electrodes W and the bit line electrodes B which cross at this cell. In fig. 10 all word lines W_B could for instance be activated and hence address all cells at the crossings with the hatched bit line electrode B as shown. A memory matrix which comprises a layer of memory material in sandwich between word and bit lines in an arrangement as shown in fig. 10 can comprise several hundred or thousands of electrodes in each direction and extend laterally over macroscopic distances (millimetres to centimetres). The thickness of each separate layer, i.e. composed of layers which form electrode layers and memory medium, will be of a magnitude of 1 μm or less. Such matrices can be stacked and form the stack in a device according to the invention and it is then obtained a monolithic structure where each single layer which forms a matrix is isolated electrically against crosstalk and interference from the other layers in the stack, such that an extremely high volumetric memory cell density is obtained.

In a high density stack of large passive matrices the number of lines in the device which are connected with suitable driver and control circuits will be very large. If the layers in the stack are completely passive with all circuits for switching, multiplexing, detection and processing located on or in a supporting substrate, can the number of direct electrical connections between individual layers in the stack and the substrate be comparable with the total number of matrix lines, i.e. word and bit lines in the device, and the problems

connected with the fabrication of such devices hence will be of paramount importance.

There shall now be given a description of a preferred method for fabrication of a device according to the invention where the separate layers are matrix-addressable devices as discussed above and where the device according to the invention hence forms a stack thereof, such that for instance a volumetric matrix-addressable memory device is obtained. The method is shown step-by-step in figs. 11a-11m, but for the case of simplicity the number of word lines is limited to 2 and the number of bit lines to 3, such that each matrix-addressable device in each single layer becomes a 2·3 matrix, in other words with at most 6 addressable cells and with a stack limited to only three layers. By using the method steps as shown in fig. 11a-11m a densely stacked matrix of passive, matrix-addressable devices can be obtained, as the series of fabrication steps provides for obtaining an electric connectivity with high density to the substrate. In the example shown the word lines in the separate layers are connected with a common conductor, while a separate set of bit lines is provided for each layer. In the subsequent figs. 11a-11m I_L denotes isolation layers, S substrate, W_L word lines and B_L bit lines, while index L respectively refers to layers L_1, L_2, L_3.

Fig. 11a shows the substrate S with respectively a bit line contact field with contact pads B_1-B_3 for respectively first to third bit lines in each layer and a word line contact field with only two contact pads W_1,W_2 for each of the word lines W_L in all layers, but before the first layer in the stack has been deposited, fig. 11b the substrate S with the first isolation layer I_{L1} to protect against electric and chemical interference between the substrate S and the thereabove provided stack, and fig. 11c how bit lines from the first layer, i.e. the first matrix-addressable device in the stack, are provided and connected with the first set of contact pads for the bit lines on the substrate S. In fig. 11d a layer M_{L1} of a functional material is shown provided, in this case a memory material, above the bit lines and which contacts these, while fig. 11e shows how word lines W_{L1} are connected with word line contacts in the substrate S. Another isolation layer I_{L2} is in fig. 11f shown provided over the first layer or the first memory device in the stack and is then provided with the bit lines B_{L2} for the second layer, such this is shown in fig. 11g. Thereabove again a memory layer M_{L2} for the second layer is provided and contacts the bit lines B_{L2}, such this is apparent from fig. 11h. Fig. 11i shows

provided word lines W_{L2}. These contact the word line W_{L1} such that common contacting for the word lines is obtained.

A new isolation layer I_{L3} for the third layer is provided as shown in fig. 11j and is provided with bit lines B_{L3} as shown in fig. 11k. Fig. 11l shows the memory layer M_{L3} for the third layer deposited over B_{L3} and it is as shown in fig. 11m provided with word lines W_{L3} which extends over the edge of each layer and forms edge connections to word lines W_{L2} on the underlying layer.

The method steps as shown in fig. 11a-11m realizes a stacked passive matrix-addressable memory device which wholly corresponds to the device according to the invention. It shall of course, be understood that the limitation of word and bit lines in the example shown in fig. 11a-11m of course, do not correspond to the realities as a device according of the invention embodied as a passive matrix-addressable memory device very well may comprise a larger number of layers and at least up to several thousand word and bit lines in each layer. For instance it has turned out to be possible to realize two-dimensional memory devices as 8000x8000 matrices, i.e. with 64 000 000 matrix-addressable memory cells, and by stacking the number of cells, of course, will increase proportionally to the number of layers in the stack such that a volumetric device according to the invention with high storage capacity and high storage density is obtained.

In the separate layers as shown in figs. 11a-11m it can besides be possible to modify the fabrication, as in reality several procedures could be used. For instance could the word lines be formed in a single step by using a method in analogy with the step shown in fig. 5a-e and correspondingly will the provision of the bit lines, e.g. as shown in fig. 11k, make it necessary that a larger number of layers must be negotiated in s single fabrication step. If this is a problem, a patterning alternative based on the geometry as shown in fig. 9a can be used or the edge connections can be formed sequentially with patching to an underlying step in analogy with the fabrication steps shown in figs. 6a-d.

Even if it is possible to combine the principles in the present invention with through-going vias according to prior art, certain essential features shall be noted which qualitatively distinguishes the two.

- In the present invention, vertical connectivity in the stack as well as intra-layer patching can be achieved in manufacturing operations after the layers in the stack have been laid down, providing increased flexibility in selecting manufacturing strategies (materials compatibility issues; customizing of devices, e.g. post stacking).

- In the present invention, no etching, drilling or similar operation is required to open connecting channels through layers in the stack.

The present invention provides realistic routes towards large-scale manufacturing of stacked devices in low-cost, high-volume operations such as reel-to-reel production of polymer-based devices.

PATENT CLAIMS

1. A memory and/or data processing device having at least two stacked layers (L) provided in a stack (1), wherein the stack (1) either forms a self-supporting structure or alternatively is provided on a substrate (2), and wherein the stack (1) comprises at least one structure staggered in at least one direction, such that steps in the staggered structure are formed by exposed portions of the separate layers (L) in the stack (1) and with a step height h corresponding to the thickness of the respective layers, characterized in that
one or more contact pads (4) are provided on each step in the staggered structure in electrical connection with memory and/or processing circuits in the respective layer (L), and that one or more electrical edge connections (3) are provided on and over the step in each layer (L) in the form of electrical conducting structures on the step and over the edge between the steps in each layer (L) and deposited on the surface of the layers (L), the electrical edge connections (3) contacting one or more contact pads (4) in the layers (L) and providing electrical connection between each layer and also between the layers and contact pads (5) provided on an optional substrate (2).

2. A memory and/or data processing device according to claim 1, characterized in that two or more contact pads (4) in one or more layers (L) are mutually connected by electrical conducting structures provided on the step in the respective layer.

3. A memory and/or data processing device according to claim 1, characterized in that the electrical edge connections (3) are provided as continuous current paths between contact pads (4) in at least three consecutive layers (L) in the stack (1) or between contact pads (4) in at least two adjacent layers (L) in the stack (1) and an optional substrate (2) adjacent to one of these layers.

4. A memory and/or data processing device according to claim 1, characterized in that the electrical edge connections (3) are provided as a patched current path between two adjacent layers (L) in the stack (1) or between an optional substrate (2) and the layer (L_1) adjacent to the substrate.

5. A memory and/or data processing device according to claim 1, characterized in that the stack (1) forms at least a part of a step pyramid structure, such that the layers (L) have different areas.

6. A memory and/or data processing device according to claim 1, characterized in that the separate layers (L) in the stack (1) are mutually displaced, such that the staggered structure comprises at least one staggered portion where the steps form an exposed portion of an upper surface in the respective layers (L) in the stack (1) and at least one staggered portion where the steps form an exposed portion of a lower surface in the respective layers (L) in the stack (1), one or more contact pads (4) on each step in each case being electrically connected with conducting structures (3) respectively provided on opposite surfaces of the layers (L).

7. A memory and/or data processing device according to claim 1, wherein the stack (1) is provided on a substrate (2), characterized in that the stack (1) forms at least a part of an inverted step pyramid-like structure, such that the area of each layer (L) increases with the distance from the substrate (2), and that overlying layers are carried over the edges of underlying layers and to rest against the substrate (2), overlying layers (L) being formed with one or more staggered portions, whereby the number of steps in the staggered portion of a layer corresponds to the number of layers located therebeneath.

8. A memory and/or data processing device according to claim 7, characterized in that one or more contact pads (5) are provided in the substrate (2) where the layers (L) rest against the substrate (2).

9. A memory and/or data processing device according to claim 1, characterized in that the side edge of each layer (L) between the steps is rounded or forms an inclined surface.

10. A method for fabrication of a memory and/or data processing device which comprises at least two layers (L) provided in a stack (1), wherein the stack (1) either forms a self-supporting structure or alternatively is provided on a substrate (2), and wherein the stack comprises at least one structure staggered in one direction, such that steps in the staggered structure are formed of exposed portions of the separate layers (L) in the stack (1) and with a step height h corresponding to thickness of the respective layers,

characterized by adding each layer in the stack in separate succeeding steps, providing each succeeding layer in the stack with an area different relative to the previous adjacent layer or displaced in relation thereto, such that the stack is formed with the at least one staggered structure in one direction, steps in the staggered structure being formed by exposed portions in the provided layers, depositing structures of conducting material on the steps in each layer, such that one or more current paths and one or more contact pads are formed on each layer, and depositing continuous and/or patched electrical conducting structures which form electrical edge connections between the contact pads on two or more layers and/or between the contact pads or one or more layers and the substrate.

11. A method according to claim 10, characterized by depositing the layers such that the stack forms at least a part of a step pyramid structure.

12. A method according to claim 10, wherein the layers (L) are provided on a supporting substrate (2), characterized by depositing the layers such that the stack forms at least a part of an inverted step pyramid structure, each overlying layer being deposited over the edge of an underlying layer and to rest against the substrate, whereby overlying layers are formed with one or more staggered portions, the number of steps in each staggered portion in a layer corresponding to the number of layers located therebeneath.

13. A method according to claim 12, characterized by providing one or more contact pads in the substrate where the layers rest against the substrate.

14. A method according to claim 10, characterized by providing the electrical edge connections in a process selected among one of the following, viz. lithography, dry etching, ink jet printing, silk printing, soft lithography, electrolysis, electrostatic deposition or in situ conversion.

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REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving Office use only

International Application No. PCT/NO 01/00113

International Filing Date 2001-03-15 (15.03.01)

PATENTSTYRET
Styret for det industrielle rettsvern

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference *(if desired) (12 characters maximum)* Opti49PCT

Box No. I TITLE OF INVENTION

Vertical electrical interconnections in a stack

Box No. II APPLICANT

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

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Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

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This person is:

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State *(that is, country)* of nationality: NO

State *(that is, country)* of residence: NO

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☒ the United States of America only ☐ the States indicated in the Supplemental Box

☐ Further applicants and/or (further) inventors are indicated on a continuation sheet.

Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as: ☐ agent ☒ common representative

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Continuation of Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

If none of the following sub-boxes is used, this sheet should not be included in the request.

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

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- [X] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality: NO

State *(that is, country)* of residence: BE

This person is applicant for the purposes of:
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- [X] the United States of America only
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- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality: NO

State *(that is, country)* of residence: NO

This person is applicant for the purposes of:
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- [X] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

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State *(that is, country)* of residence: SE

This person is applicant for the purposes of:
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Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

This person is:
- [ ] applicant only
- [ ] applicant and inventor
- [ ] inventor only *(If this check-box is marked, do not fill in below.)*

State *(that is, country)* of nationality:

State *(that is, country)* of residence:

This person is applicant for the purposes of:
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Box No.V DESIGNATION OF STATES

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Check-box reserved for designating States which have become party to the PCT after issuance of this sheet:

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Precautionary Designation Statement: In addition to the designations made above, the applicant also makes under Rule 4.9(b) all other designations which would be permitted under the PCT except any designation(s) indicated in the Supplemental Box as being excluded from the scope of this statement. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit. *(Confirmation (including fees) must reach the receiving Office within the 15-month time limit.)*

Box No. VI PRIORITY CLAIM ☐ Further priority claims are indicated in the Supplemental Box.

Filing date of earlier application (day/month/year)	Number of earlier application	Where earlier application is: national application: country	regional application:* regional Office	international application: receiving Office
item (1) 15 March 2000 (15.03.2000)	20001360	NO		
item (2)				
item (3)				

☒ The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) *(only if the earlier application was filed with the Office which for the purposes of the present international application is the receiving Office)* identified above as item(s): (1)

** Where the earlier application is an ARIPO application, it is mandatory to indicate in the Supplemental Box at least one country party to the Paris Convention for the Protection of Industrial Property for which that earlier application was filed (Rule 4.10(b)(ii)). See Supplemental Box.*

Box No. VII INTERNATIONAL SEARCHING AUTHORITY

Choice of International Searching Authority (ISA) *(if two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used)*: ISA/SE

Request to use results of earlier search; reference to that search *(if an earlier search has been carried out by or requested from the International Searching Authority)*:
Date *(day/month/year)* Number Country *(or regional Office)*

Box No. VIII CHECK LIST; LANGUAGE OF FILING

This international application contains the following **number of sheets**:

request	:	4
description (excluding sequence listing part)	:	12
claims	:	2
abstract	:	1
drawings	:	12
sequence listing part of description	:	
Total number of sheets	:	31

This international application is accompanied by the item(s) marked below:

1. ☐ fee calculation sheet
2. ☐ separate signed power of attorney
3. ☐ copy of general power of attorney; reference number, if any:
4. ☐ statement explaining lack of signature
5. ☐ priority document(s) identified in Box No. VI as item(s):
6. ☐ translation of international application into (language):
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9. ☐ other *(specify)*:

Figure of the drawings which should accompany the abstract: 1a, 1b

Language of filing of the international application: ENGLISH

Box No. IX SIGNATURE OF APPLICANT OR AGENT

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Geirr I. Leistad
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/NO 01/00113

A. CLASSIFICATION OF SUBJECT MATTER

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5093708 A (ALLEN L. SOLOMON), 3 March 1992 (03.03.92), column 2, line 3 - line 61; column 5, line 65 - column 6, line 16, figure 7, abstract	1-7
A	US 5502289 A (HEM P. TAKIAR ET AL), 26 March 1996 (26.03.96), figures 6,8, abstract	1-7
A	EP 0522518 A2 (HUGHES AIRCRAFT COMPANY), 13 January 1993 (13.01.93), figure 3, abstract	1-7

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
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INTERNATIONAL SEARCH REPORT

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Patent Abstracts of Japan, abstract of JP 58-178547 A (MATSUSHITA DENKI SANGYO K.K.), 20 January 1984 (20.01.84), Vol. 8, No. 13 (E222) --	1-7

INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5093708 A	03/03/92	WO 9203844 A	05/03/92
US 5502289 A	26/03/96	DE 69325749 D,T	17/02/00
		EP 0575051 A,B	22/12/93
		JP 6037250 A	10/02/94
		US 5422435 A	06/06/95
		US 5495398 A	27/02/96
EP 0522518 A2	13/01/93	AU 656595 B	09/02/95
		AU 1947592 A	21/01/93
		CA 2073363 A	10/01/93
		IL 102397 A	30/03/95
		JP 5259375 A	08/10/93
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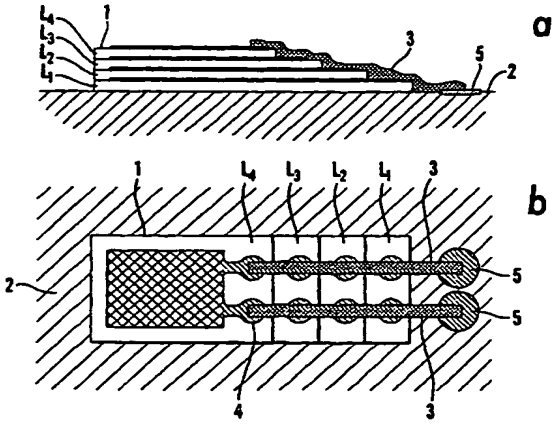
(54) Title: VERTICAL ELECTRICAL INTERCONNECTIONS IN A STACK



(57) Abstract: In a memory and/or data processing device having at least two stacked layers which are supported by a substrate or forming a sandwich self-supporting structure, wherein the layers comprise memory and/or processing circuitry with mutual connections between the layers and/or to circuitry in the substrate, the layers are mutually arranged such that contiguous layers form a staggered structure on at least one edge of the device and at least one electrical edge conductor is provided passing over the edge on one layer and down one step at a time, enabling the connection to an electrical conductor in any of the following layers in the stack. A method for manufacturing a device of this kind comprises steps for adding said layers successively, one layer at a time such that the layers form a staggered structure and for providing one or more layers with at least one electrical contacting pad for linking to one or more interlayer edge connectors.

WO 01/69679 A1

Vertical electrical interconnections in a stack

The present invention concerns a memory and/or data processing device having at least two stacked layers that overlap each other partially or completely, wherein said layers are supported by a substrate or alternatively forming a sandwiched self-supporting structure of such stacked layers, and wherein at least two layers in the stack comprise memory and/or processing circuitry that connects electrically to memory and/or processing circuitry in at least one other layer and/or substrate; and a method for manufacturing a device of this kind.

Modern electronic microcircuits are typically built layer by layer on silicon chips in a series of process steps where insulating layers separate layers containing metallic, insulating and semiconducting materials that are patterned and processed by various deposition and etching techniques. Integral to the ensuing architectures are electrical connections between components and sub-circuits which are located in the substrate and in layers on top of the substrate. These connections, termed vias, are typically in the form of metallic posts or wires that penetrate through one or more layers of intervening material separating the components to be connected. Such vias are either made during the layer-building process or they are inserted through already existing layers by creating channels through the layers (by e.g. etching), followed by filling metal plugs into the channels.

Present-day state-of-the-art silicon chips may involve 20-30 masking steps, and the number of separate layers containing patterned metal intra-layer leads that connect directly or indirectly to a via is typically 3-5. Each via requires a certain amount of real estate associated with it in each layer that is traversed or connected: In addition to the metal cross section of the via itself, there must be allocated a buffer zone around it which insulates the via from adjacent circuitry that shall not be in immediate contact with the via, and allowance must be made for the finite precision with which the patterning in each layer can be made as well as registration accuracy of patterning masks.

The above referred prior art has generally proved adequate for devices built on silicon substrates as referred above, where the number of layers and vias is low to moderate, and where ultra-high precision lithography is an integral part of the chip-making process. However, vias represent a considerable complicating feature in the overall manufacturing process, with impact on

yield and costs. Furthermore, it is expected that entirely new types of device architectures and manufacturing methods for electronic data processing and -storage shall emerge in the next few years as serious contenders for large commercial segments. A common feature of such new architectures shall be that they incorporate thin-film electronics in dense stacks containing very large numbers of layers. In many instances, these devices shall be manufactured by high-volume technologies such as roll-to-roll processing on thin polymer substrates. In this context, traditional via connection technologies shall be totally inadequate, technically as well as cost-wise.

It is a major object of the present invention to provide methods and technical solutions whereby electrical interconnects can be created between layers and/or between layers and an underlying substrate, in memory and/or processing devices that incorporate a stack containing two or more sheet- or film-like functional parts that partially or completely overlap each other.

It is also an object of the present invention to provide such methods and technical solutions that can be implemented in cases where the number of such sheet- or film-like functional parts becomes large, typically exceeding 5-10.

It is a further object of the present invention to provide such methods and technical solutions that can be implemented in cases where such sheet- or film-like functional parts are manufactured and devices assembled by high-volume, low cost technologies.

The above-mentioned objects and further features and advantages are realized according to the invention with a device which is characterized in that said layers are arranged in relation to each other such that contiguous layers form a staggered structure on at least one edge of said device, the edge of at least two layers in said structure forming a set of angular or sloped steps where each step has a height corresponding to the thickness of each layer, and that at least one electrical edge conductor is provided passing over the edge of one layer and down one step at a time, enabling the connection to an electrical conductor in any of the layers following in the staggered structure; and a method which is characterized by comprising steps for adding said layers successively, one layer at a time such that the layers form a staggered structure, and for providing each layer with at least one electrical contacting pad for linking to one or more interlayer edge connectors.

In an advantageous embodiment of the device according to the invention comprises at least one electrical conductor provided passing over the edge of said staggered structure and connecting electrically to in-layer conductors in two or more and up to a plurality of contiguous layers, negotiating one step at a time.

In this connection it is preferred that said in-layer conductors form electrical connections between electrical conductors negotiating the step up to the contiguous layer above and/or down to the contiguous layer below.

In a first advantageous embodiment of the method according to the invention said layers are provided on a supporting substrate and forming said staggered structure is formed as a step pyramid.

In a second advantageous embodiment of the method said layers are provided on a supporting substrate, said staggered structure is formed as an inverted pyramid, each of said layers connecting to said substrate via said electrical edge connectors negotiating a single step.

Finally, in the method according to the invention it is considered advantageous forming said edge connectors in a process selected among one of the following, viz. lithography, dry etching, inkjet printing, silk screen printing, soft lithography, electrolysis, or in situ conversion

The invention shall now be described in detail, with reference to the accompanying drawings, where

fig.1a shows a side view of a generic device, termed of the "pyramid" type here. It consists of stacked functional units located on separate but mutually adhering sheets or film layers mounted on a base substrate. Circuitry on the top surface of a given layer is electrically connected to localized contacting pads on an exposed edge area of that sheet.

Figs. 1b and 1c show top views of two alternative architectures consistent with the side view in Fig.1a. In Fig.1b the structure is stepped in one direction, in Fig.1c in two.

Fig.2 shows an analogous structure to that shown in Fig.1a, but now the edge of each layer is sloped or tapered

Fig.3 shows an analogous structure to that shown in Fig.1c, buit now multiple contacting pads are provided on each step, yielding possibilities for patching of intra- and inter-layer connections.

Figs.4a-c show analogous structures to those in Fig.1a, but in this case the stack is self-supporting, i.e. there is no supporting substrate.

Fig.4d also shows a self-supporting structure. In this case both sides of each layer can be accessed separately.

Figs.5a-e show an example of manufacturing steps for creating structures of the type shown in Fig.1a.

Figs.6a-d illustrate an alternative example to that in Figs.5a-e of manufacturing steps for creating structures of the type shown in Fig.1a. In this case, edge connections are made one step at a time, to conform with e.g. limited depth of field when employing high resolution optical lithography in making of the edge connections.

Fig.7 shows a side view of a generic device, termed of the "inverted pyramid" type here. As with the pyramid type devices, it consists of stacked functional units located on separate but mutually adhering sheets mounted on a base substrate. In this case, however, the area of each layer in the stack increases as the distance from the substrate increases. Each layer has its separate access to dedicated landing pads in/on the substrate.

Figs.8a-g show an example of manufacturing sequence for creating structures of the type shown in Fig.7.

Figs.9a-b show, for the "pyramid" and "inverted pyramid" case, respectively, how patterning of connectors across a stack edge can be achieved with moderate depth of field requirements and correspondingly high resolution, by patterning at an oblique angle to the planes of the layers in the stack.

Fig. 10 shows a prior art passive matrix arrangment.

Fig.11a-m shows an example of manufacturing steps in making a stacked, passive matrix addressed memory. For simplicity, the device shown has only 2 word-lines, 3 bit-lines and 3 memory layers.

According to the present invention, electrical connections between layers in a stack and/or between such layers and a supporting substrate are created by negotiating a stepped or sloped edge of the stack, as shown schematically in figs. 1a-c.

Fig.1a shows a side view of a stack, where common connector provides electrical contact between an exposed contact pad in the substrate and exposed conductors on the steps of the stack.

Fig.1b shows a top view of the stack in fig.1a, with exposed contacting pads in each given layer being linked electrically by in-layer conductors to specific parts of the circuitry in that layer. In the figure, the circuitry in the top layer is shown as a cross-hatched field. The latter may of course represent one or more networks of physically separated components or circuits, and the two connecting paths to the substrate shown in the figure couple to different parts of the in-layer circuitry.

Fig.1c shows a top view of a different stack which also is compatible with the side view in fig.1a. In this case, the stack is stepped in two mutually orthogonal directions, providing increased exposed step area for coupling purposes as well as spreading out the contacting pad locations on the substrate. Clearly, a number of alternatively stepped structures in 3, 4, 5 etc. directions are possible by direct extension of the principles described here.

In order to reduce the risk of breaking the electrical continuity at the point where the connector climbs a given step, that step may be rounded at the edge, or shaped as a gradual slope, cf. fig. 2.

The generic edge connectivity shown in figs. 1 and 2 may be achieved either in a single electrode deposition step (cf. fig. 5e) or in a sequence of deposition operations (cf. fig. 6b-d). In the latter case, each deposition operation involves negotiating a smaller part of the total edge height, e.g. a single step in the edge structure, and continuity of the electrical connection across several steps is achieved by overlap between successively deposited electrodes.

Each layer in the stack may itself be a sandwich of sub-layers containing electrical conduits, active circuitry and functional materials, e.g. memory substances for data storage purposes. Depending on the chosen technologies, each layer may be prefabricated on a supporting film member before being built into the stack, or it may be constructed by one or a series of deposition processes onto the surface of the stack itself. In the former case, each layer may have a thickness whose lower limit shall be defined by the structural strength of the supporting film in relation to the stress it is subjected to during the prefabrication and stack addition processes. In the latter case, the layer thickness may be much less, down to monolayer coverages.

Although it is possible to combine the principles of the present invention with prior art-type penetrating vias, one should note certain salient features which set the two qualitatively apart:

- In the present invention, vertical connectivity in the stack as well as intra-layer patching can be achieved in manufacturing operations after the layers in the stack have been laid down, providing increased flexibility in selecting manufacturing strategies (materials compatibility issues; customizing of devices, e.g. post stacking).

- In the present invention, no etching, drilling or similar operation is required to open connecting channels through layers in the stack.

- The present invention provides realistic routes towards large-scale manufacturing of stacked devices in low-cost, high-volume operations such as roll-to-roll production of polymer-based devices.

As thin-film based active circuitry employing inorganics, oligomers or polymers enters the mainstream of commercial electronics, it is expected that stacked devices with "smart" layers, i.e. layers that possess individual processing capabilities, shall become ubiquitous. In addition to enhancing the possibilities inherent in the stacking concept, this implies that bus-type edge connections may carry messages that are distributed globally across the stack and picked up selectively by those layers they are intended for. On the other hand, the interconnect concepts of the present invention may involve stacks that contain sheets or layers without decoding circuitry, in which case dedicated edge connections to those sheets may have to be provided. An extreme case of the latter is where all layers are "dumb" and where each

layer has dedicated electrical connections to driving circuitry on a supporting substrate or circuitry at a cable-connected location elsewhere. In what follows, these different aspects of possible electronic capabilities in individual layers shall not be treated in any further detail, since the appropriate choices of solutions according to the present invention will be obvious to the skilled person.

Before turning to more detailed discussions related to preferred embodiments, certain generic aspects of the present invention shall be pointed out:

Examples of these are shown in figs.1, 2 and 3. The edge connections on a given layer in a stack are established by allocating an edge area of that layer for contacting purposes, the layers in the stack being mutually arranged in a series of steps. The stack may be stepped in one direction only, as shown in fig. 1b, or it may be stepped in two or more directions (cf., e.g. fig. 1c). These steps are exposed during the manufacturing of contacts, but may subsequently be protected by coating, etc.

Application of inter-layer and/or layer-to-substrate contact lines may be performed by a range of techniques, ranging from high-volume, low-cost to precision, high-cost. If precision is less important than cost, printing techniques may be preferred (ink-jet, silk screen, stamping, electrostatic deposition), with the proviso that the edge conductors thus created must be able to negotiate the steps in the stack. In high-density devices, edge connectors must be defined with high precision, not only where they shall connect to a small contacting area on the step of a given layer, but also where they climb the edge of the stack and shall encroach as little as possible to each side. Thus, a single edge of a stack may well contain hundreds or thousands of parallel conductors climbing up the side (for practical reasons, only a single or a few conducting lines are shown in the figures here).

Techniques for creating edge connectors with high precision include lithographic techniques with wet or dry etching, as well as particle milling, high precision stamping such as "soft lithography" and electrolysis. Common to most high resolution techniques is a restricted depth of field, limiting the height of each step and/or the number of steps that can be bridged electrically in a single manufacturing step. In such cases, a single application of a

common conductor (power; bus...) may be employed as shown in fig. 5, where:

Fig. 5a shows the substrate before building of the stack, with a circuit connecting to contacting pads.

Fig. 5b shows how an insulating layer masks off the parts of the substrate that might interfere chemically or electrically with the stack, leaving the contacting pads exposed. A first-layer circuit has been applied onto the insulating layer, with contacting pads near the edge.

Fig. 5c shows the situation following application of a second insulating layer and subsequent circuitry with connecting pads near the edge.

Fig. 5d shows the stack after application of a third insulating layer and circuitry, with exposed contact pads arranged in a sequence along the staircase edge.

Fig. 5e shows how a conducting line has been applied along each row of connecting pads on the steps, linking these pads to the connecting pads in the substrate.

The single-step application of inter-layer and layer-substrate connections can be supplanted by a stepwise approach as shown in figs. 6a-d:

Fig. 6a shows a substrate with circuitry and connecting pads, in analogy with Fig.5a.

Fig. 6b shows how an insulating layer has been applied, with circuitry and connecting pads on top.

Fig. 6c shows how an electrical connection has been established between connecting pads in the substrate and corresponding ones at the edge of the first layer in the stack.

Fig. 6c shows the situation after a second insulator layer with circuitry on top has been applied, the latter being connected via connecting pads to the exposed conductors on the step below.

Fig. 6d likewise shows how a third layer in the stack has been established, with electrical links to the layer below and thence to the substrate.

In this way, only the height of each step is negotiated in each contacting operation, which can be repeated ad libitum to achieve any desired total stack height. An alternative approach is illustrated in figs. 9a-b: Here, the steps on a side of the stack are arranged so as to present a linear slope. As can be seen, the required depth of field for application of conductors spanning the whole height of the stack can be made very small by attacking the edge at an oblique angle. A regular step height is not required, cf. fig. 9a.

In order to maximize the usable area of the layers in the stack, the area on any given layer occupied by the exposed part of the step should be kept small, but this must be weighed against the ease of manufacturing the device: A shallow step imposes closer tolerances on the contacting procedures, and steepens the edge slope of the stack. The latter aspect may prove negative in certain cases where it is desired to create edge connections by application of conductors at a skew angle (cf. references to figs. 9a-b, above). In the limiting case where steps become infinitely shallow, the stack shall have a straight edge, and circuitry in a given layer must then be accessed by electrical wiring that extends to the edge of that layer and provides exposed electrical contact material laterally from that edge.

Please refer to fig. 7. In this case, the stack is built layer by layer on a substrate which provides physical support and has on its surface electrical contacting areas as shown. Each subsequent layer extends beyond the previous one at the stepped edge, typically causing the total area of each layer to increase with the distance from the substrate. In addition to providing each layer with direct access to possible driving circuitry in the substrate, as can be the case when the substrate is a chip of silicon, electrical conduits in the substrate may connect separate layers in the stack electrically to each other via the contacting pads shown.

An example of a manufacturing sequence for a stack of the inverted pyramid type is shown in figs. 8a-g, wherein specifically

fig. 8a a substrate with connecting pads,

fig. 8b how an insulating layer has been added, masking the part of the substrate to be covered by the stack, but leaving the contacting pads exposed,

fig. 8c the situationafter application of a set of electrodes in the first stack layer connecting to the first row of contacting pads on the substrate,

fig. 8d how a second insulating layer masks off the first-layer electrodes, leaving the second-layer and subsequent-layer electrodes exposed on the substrate,

fig. 8e how a second-layer set of electrodes have been applied, climbing up two steps from the connecting pads on the substrate,

fig. 8f the situation after a third insulating layer has been applied, leaving the third-layer connecting pads in the substrate exposed, and

fig. 8g finally how a set of electrodes has been applied, providing electrical connections to the appropriate connecting pads in the substrate.

As can be observed, the latter procedure provides separate access to individual layers in the stack, as opposed to the example shown in Figs. 5 and 6.

As illustrated in figs. 4a-d, stacks may be formed without a supporting substrate, having properties that can be deduced by trivial extension of those discussed in connection with the substrate based variants above. A special aspect of self-supporting structures is increased access to exposed edges, providing opportunities for two-sided contacting as illustrated in fig. 4d.

A passive matrix arrangement is shown in fig.10: It provides a simple, dense architecture for providing addressed cells located at the crossing points between the word lines and the bit lines, and has been used in applications that include memory devices and displays.

For concreteness, the present example of a preferred embodiment shall focus on the case of memory devices, but the general principles shall be applicable to other types of devices also:

The crossing electrodes sandwich a global layer of memory material, a memory cell being formed in the volume between each crossing of a word- and a bit-line. A given cell can be written to, read and erased by activating the word- and bit-line electrodes crossing at that cell (in fig. 10, the activated lines are shown in a darker shade). A memory matrix containing a sheet of memory material sandwiched between word- and bit-lines may contain hundreds or thousands of such lines in each direction and extend laterally across macroscopic distances (millimeters to centimeters). The thickness of this structure, however, is typically very small, of the order of a micrometer

and less. By stacking such matrices on top of each other in a monolithic structure where each layer containing a matrix is insulated electrically against cross-talk interference from other layers in the stack, extremely high volumetric densities of memory cells can be achieved.

In a high-density stack of large matrices, the number of matrix lines in the device that must be connected to appropriate driving circuitry shall be very large. If the layers in the stack are passive, with all active circuitry for switching , multiplexing, sensing or processing located in the supporting substrate, the number of direct electrical connections between individual layers in the stack and the substrate may become comparable to the total number of matrix lines in the device, and manufacturing issues shall be of paramount importance.

Fig. 11a-m shows an example of how a dense stack of passive matrix devices can be manufactured in a series of manufacturing steps providing high density electrical connectivity to the substrate. In this example, corresponding wordlines in separate layers are connected to a common conductor, while a separate set of bit-lines is provided for each layer.

Fig. 11a shows the substrate prior to deposition of the stack, with contacting pads exposed.

Fig. 11b shows the substrate with an insulating layer to protect against electrical or chemical interference between substrate and stack.

Fig. 11c shows how bit-lines for the first layer in the stack have been laid out, connecting to the first row of bit-line connecting pads in the substrate.

Fig. 11d shows how a film of functional material, in this case a film with memory capability, has been deposited on top of the bit-lines.

Fig. 11e shows how the word-lines have been laid out, connecting to the row of word-line connecting pads in the substrate.

Fig. 11f shows the situation after an insulating layer has been applied, masking off the first row of bit-line connecting pads in the substrate and completing the first memory device in the stack.

Fig. 11g shows how the bit-lines of the second memory device have been applied so as to connect to the second row of bit-line pads in the substrate.

Fig. 11h shows how the film with memory capability has been applied on top of the bit-lines.

Fig. 11i shows how the word-lines have been applied, and connected to the exposed word-line segments in the layer below, thereby achieving contact to the contacting pads in the substrate.

Fig. 11j shows how an insulating film has been applied, masking off the second row of bit-line connecting pads in the substrate.

Fig. 11k shows how the complement of bit-lines in the third memory matrix of the stack have been applied, connecting to the third row of bit-line connecting pads in the substrate.

Fig. 11 l shows how the film with memory capability has been applied on top of the bit-lines.

Fig. 11m shows finally how the third memory matrix device in the stack is supplied with bit-lines that are connected to the exposed word-line segments in a layer below, providing electrical contact down to the word-line contacting pads in the substrate.

As will be apparent, the above detailed description of manufacturing steps represents but one amongst several alternative procedures according to the present invention that can be employed to create a stacked series of memory matrices. Thus, it might be preferable in certain instances to create the word-line in a single step, by procedures analogous to those shown in figs. 5a-e. Likewise, the application of bit-lines as shown in fig.11k implies that a number of layers must negotiated in a single manufacturing step. If this represents a problem, alternatives exist such as illustrated in fig.9b, or sequential connections with patching to a lower step may be used in analogy with that shown in figs. 6a-d.

PATENT CLAIMS

1. A memory and/or data processing device having at least two stacked layers that overlap each other partially or completely, wherein said layers are supported by a substrate or alternatively forming a sandwiched self-supporting structure of such stacked layers, and wherein at least two layers in the stack comprise memory and/or processing circuitry that connects electrically to memory and/or processing circuitry in at least one other layer and/or said substrate,
characterized in that
said layers are arranged in relation to each other such that contiguous layers form a staggered structure on at least one edge of said device, the edge of at least two layers in said structure forming a set of angular or sloped steps where each step has a height corresponding to the thickness of each layer, and that
at least one electrical edge conductor is provided passing over the edge of one layer and down one step at a time enabling the connection to an electrical conductor in any of the layers following in the staggered structure.

2. A memory and/or data processing device according to claim 1, characterized in that said
at least one electrical conductor is provided passing over the edge of said staggered structure and connecting electrically to in-layer conductors in two or more and up to a plurality of contiguous layers, negotiating one step at a time.

3. A memory and/or data processing device according to claim 2, characterized in that
said in-layer conductors form electrical connections between electrical conductors negotiating the step up to the contiguous layer above and/or down to the contiguous layer below.

4. A method for manufacturing a memory and/or data processing device having at least two stacked layers that overlap each other partially or completely, wherein said layers are supported by a substrate or alternatively forming a sandwiched self-supporting structure of such stacked layers, and wherein at least two layers in the stack comprise memory and/or processing circuitry that connects electrically to memory and/or processing circuitry in at least one other layer and/or substrate, and wherein the method is

characterized by
comprising steps for adding said layers successively, one layer at a time such that the layers form a staggered structure and for providing one or more layers with at least one electrical contacting pad for linking to one or more interlayer edge connectors.

5. A method according to claim 4,
characterized by providing said layers on a supporting substrate, and forming said staggered structure as a step pyramid.

6. A method according to claim 4,
characterized by
providing said layers on a supporting substrate and forming said staggered structure as an inverted pyramid, each of said layers connecting to said substrate via said electrical edge connectors negotiating a single step.

7. A method according to claim 4,
characterized by
forming said edge connectors in a process selected among one of the following, viz. lithography, dry etching, inkjet printing, silk screen printing, soft lithography, electrolysis, electrostatic deposition, or in situ conversion.

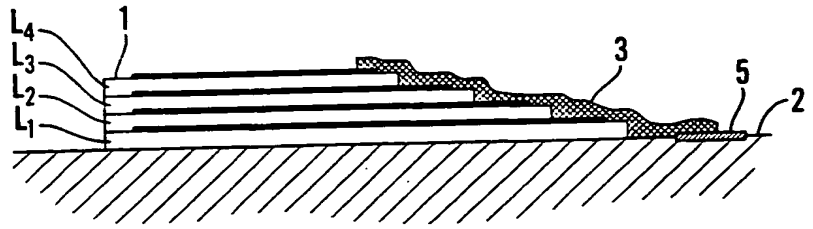


Fig.1a

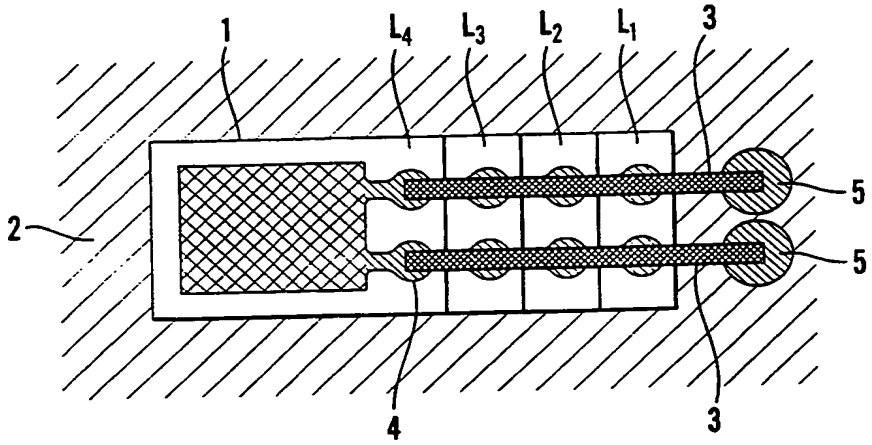


Fig.1b

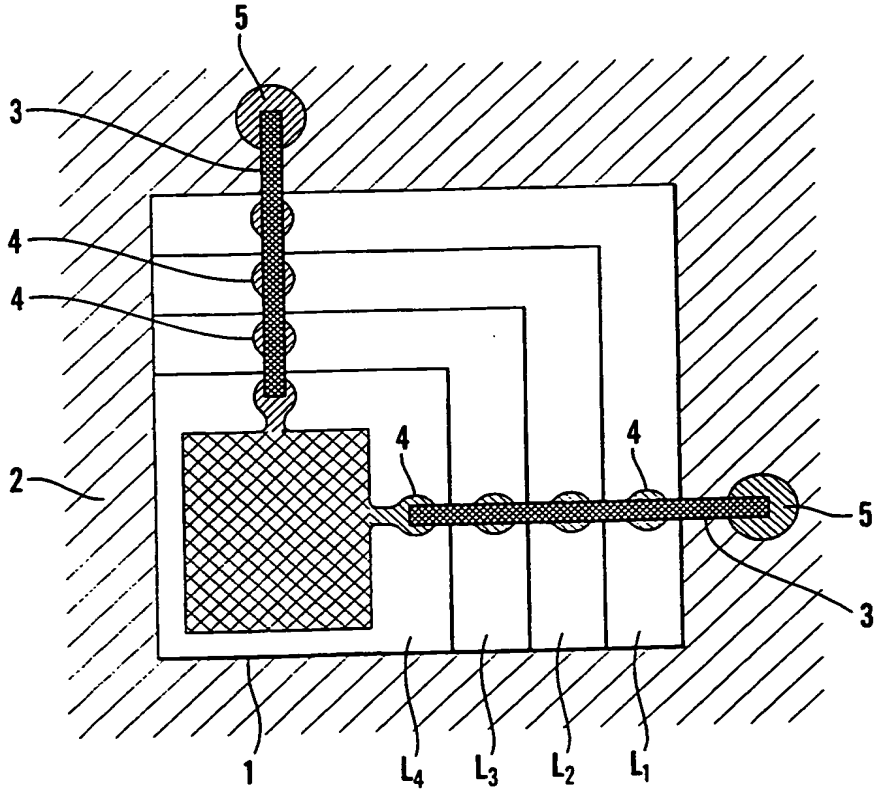


Fig.1c

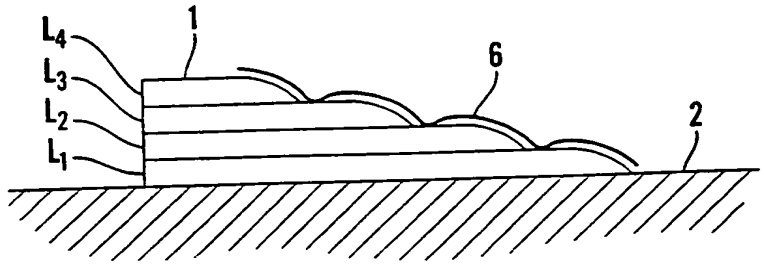


Fig.2

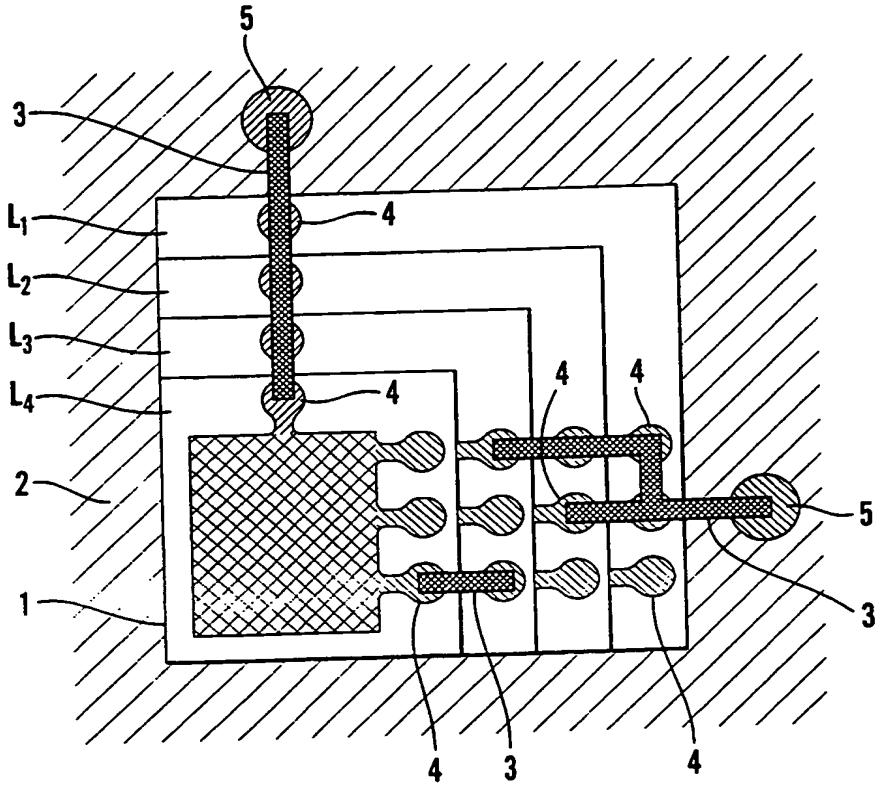


Fig.3

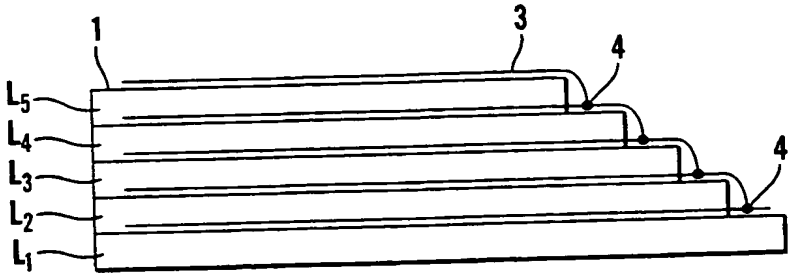


Fig.4a

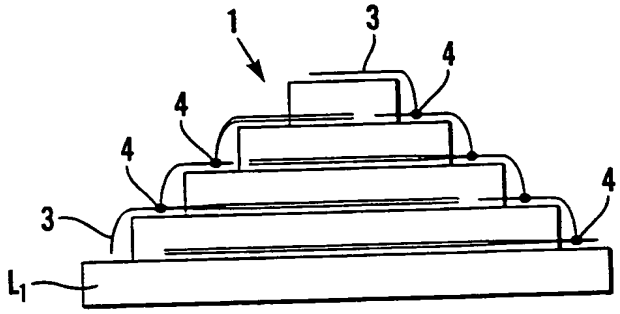


Fig.4b

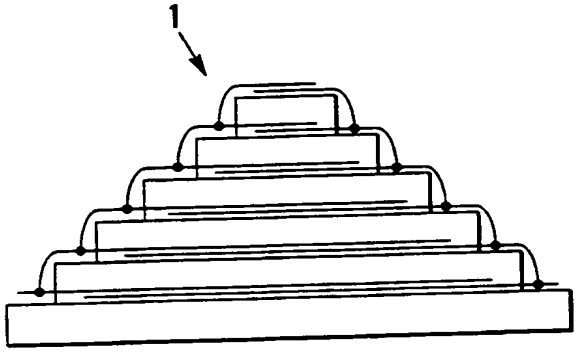


Fig.4c

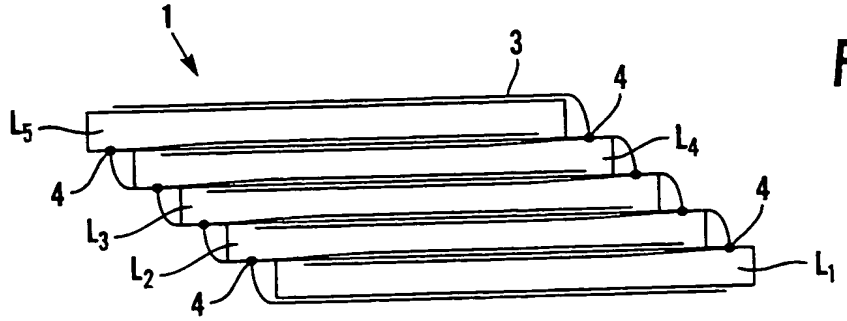


Fig.4d

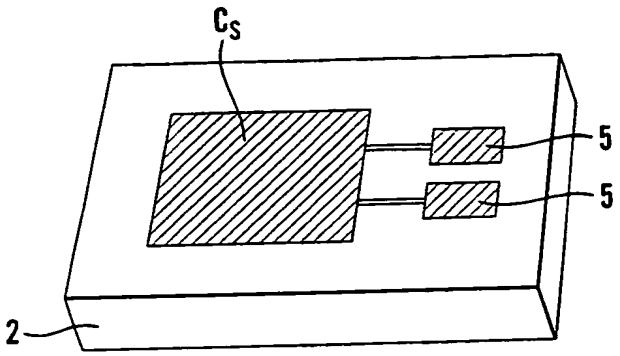


Fig.5a

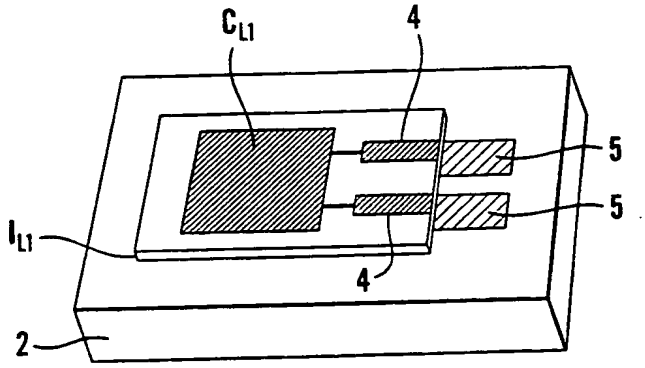


Fig.5b

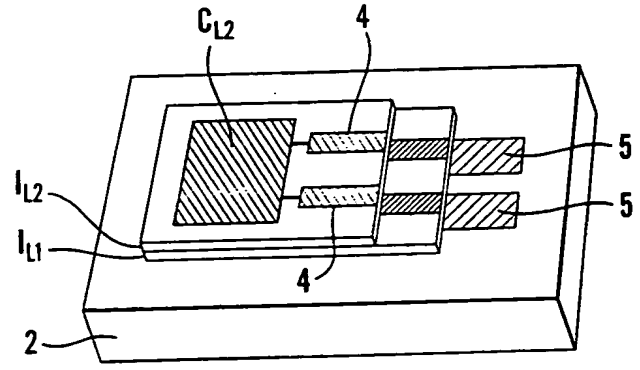


Fig.5c

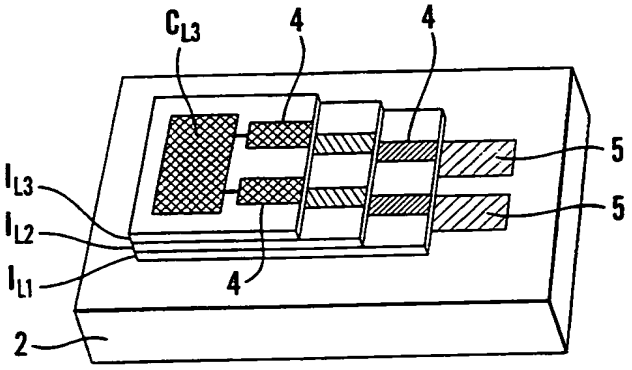


Fig.5d

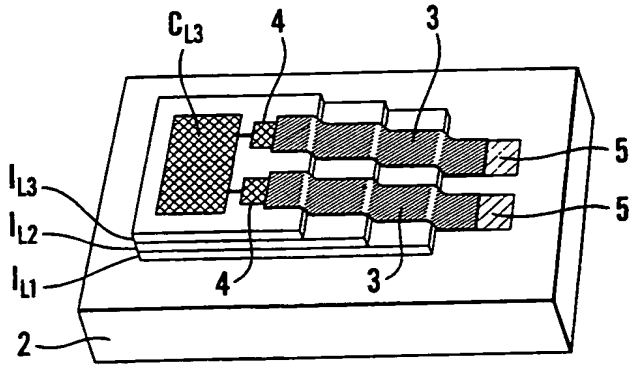


Fig.5e

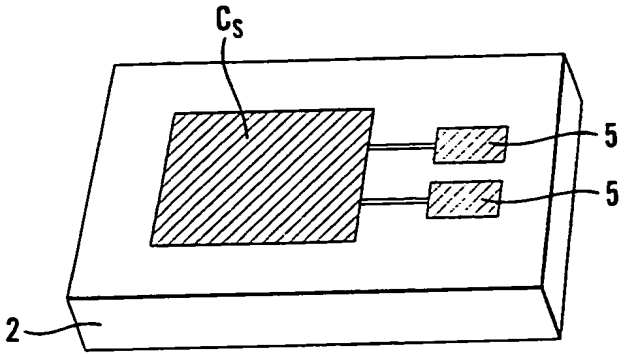


Fig.6a

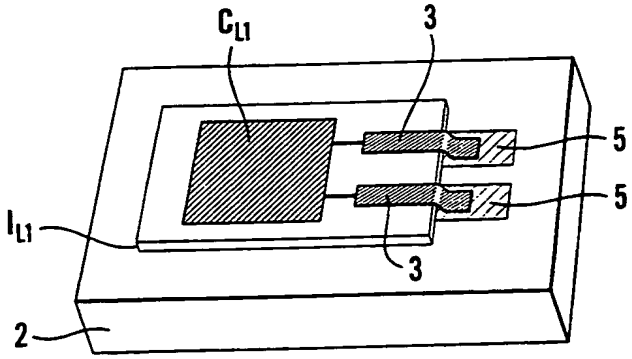


Fig.6b

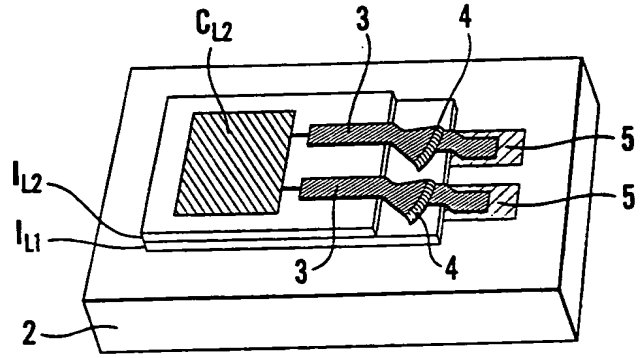


Fig.6c

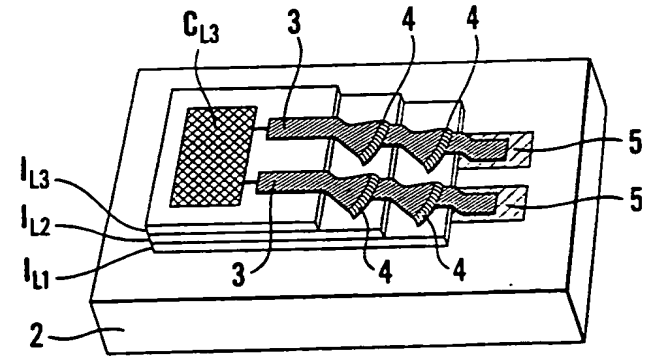
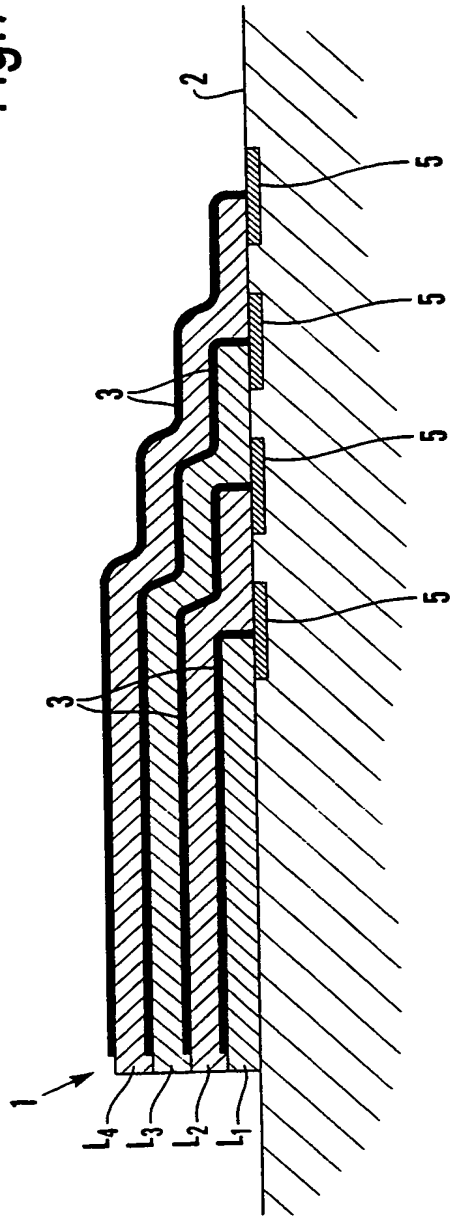


Fig.6d

Fig.7



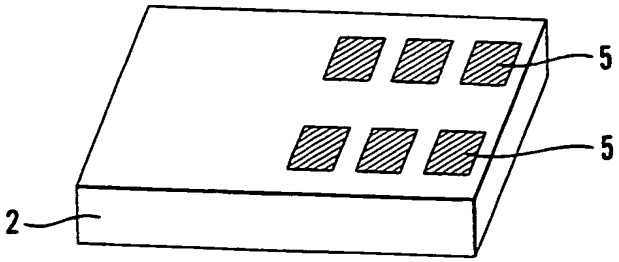


Fig.8a

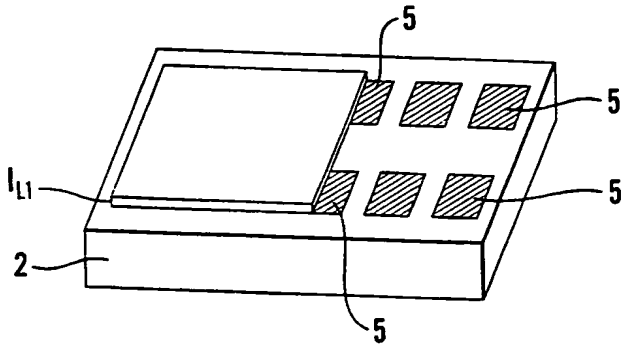


Fig.8b

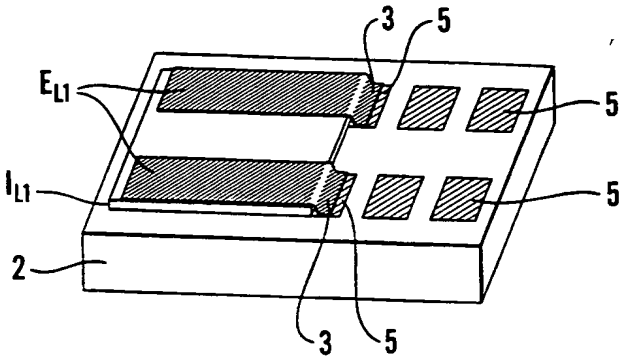


Fig.8c

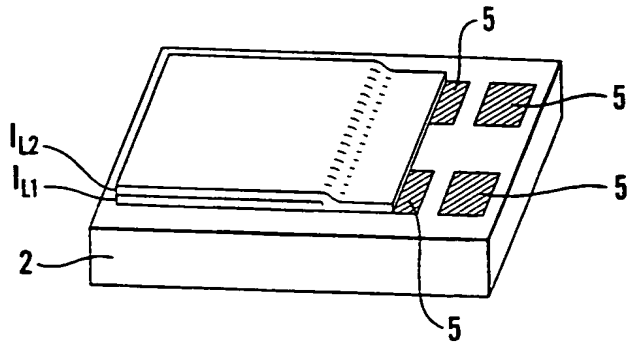


Fig.8d

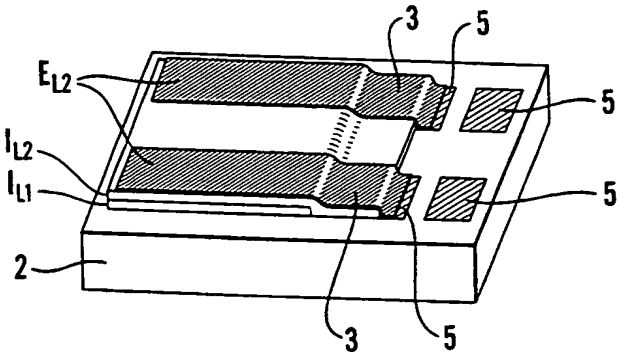


Fig.8e

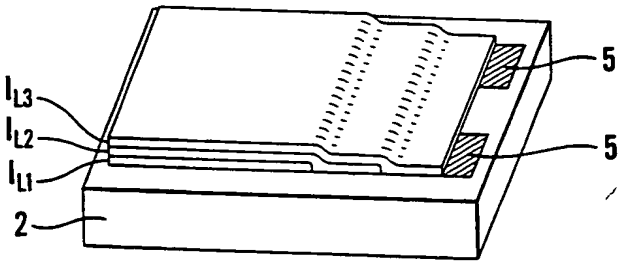


Fig.8f

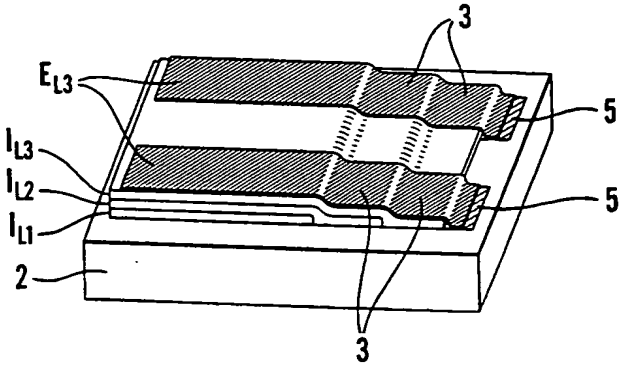


Fig.8g

Fig.9a

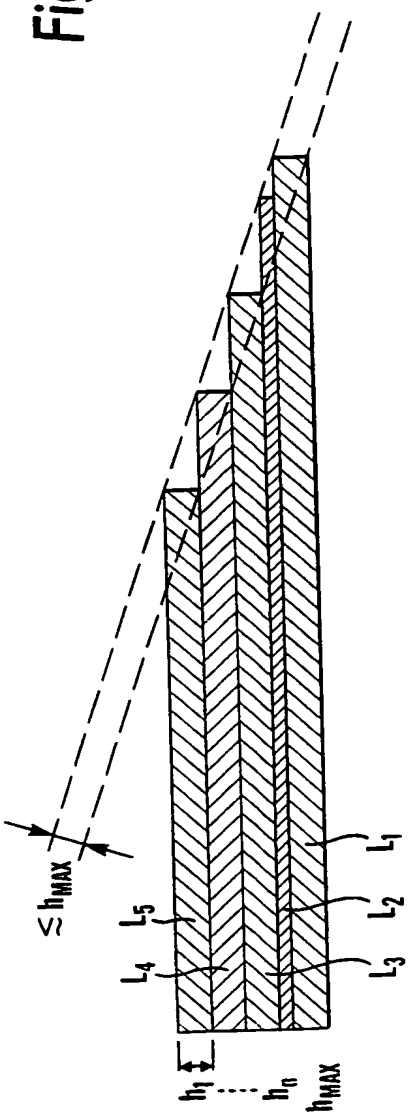
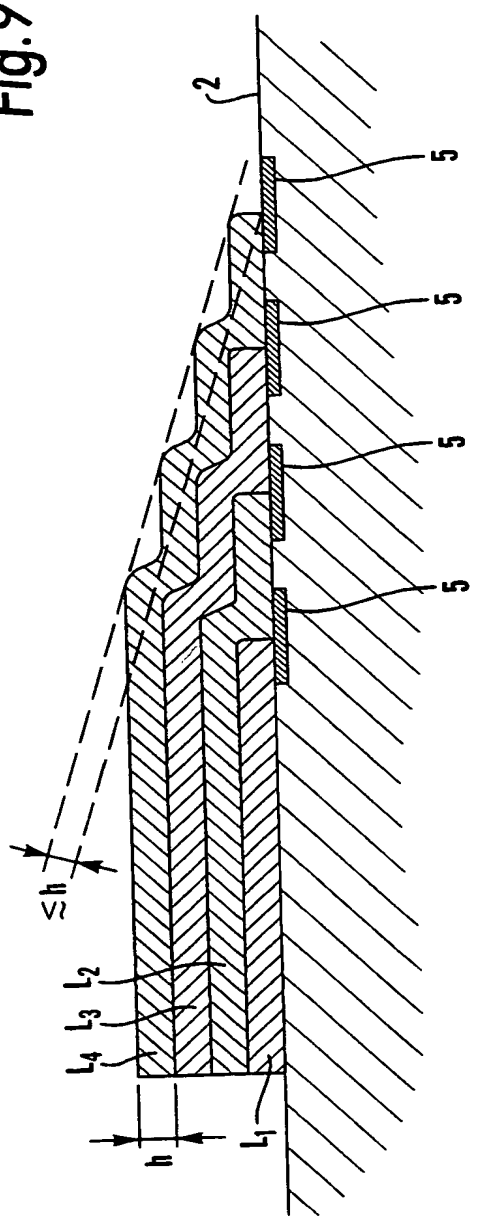


Fig.9b



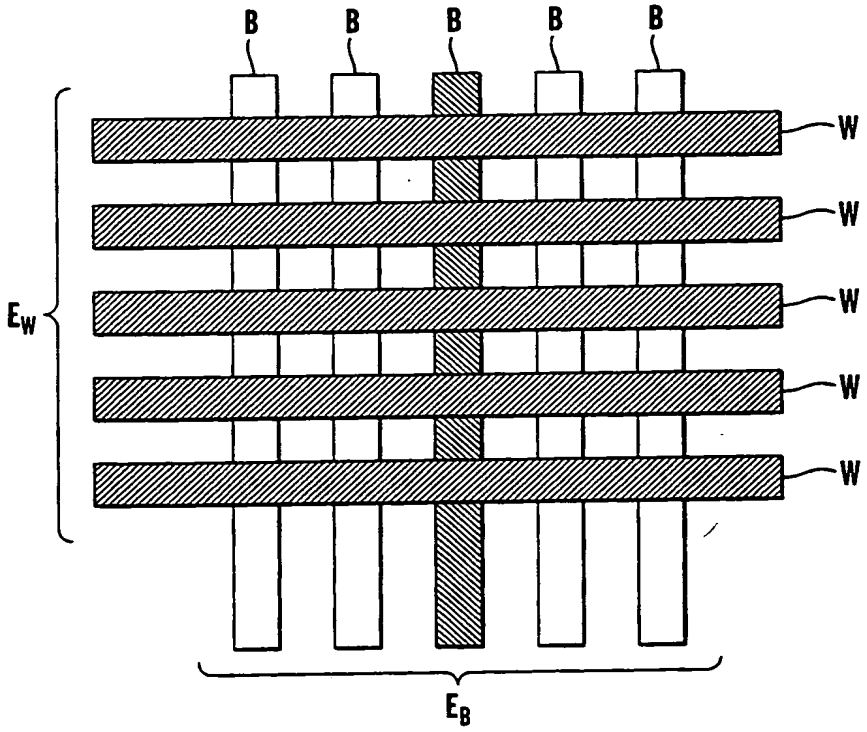


Fig.10

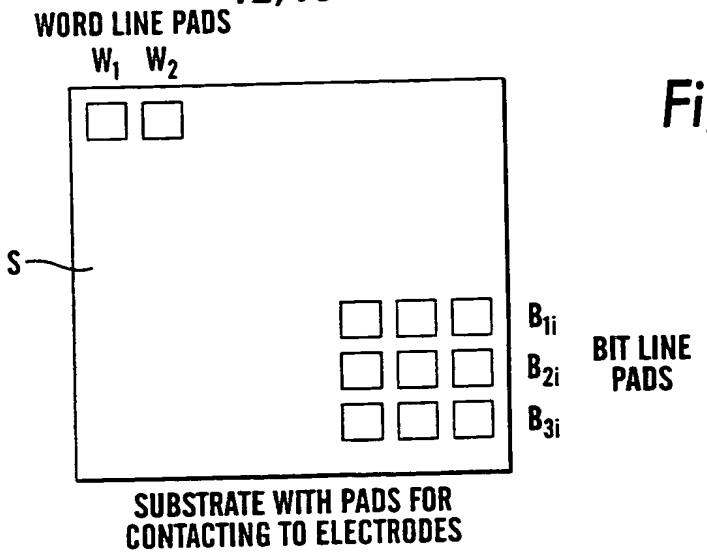


Fig.11a

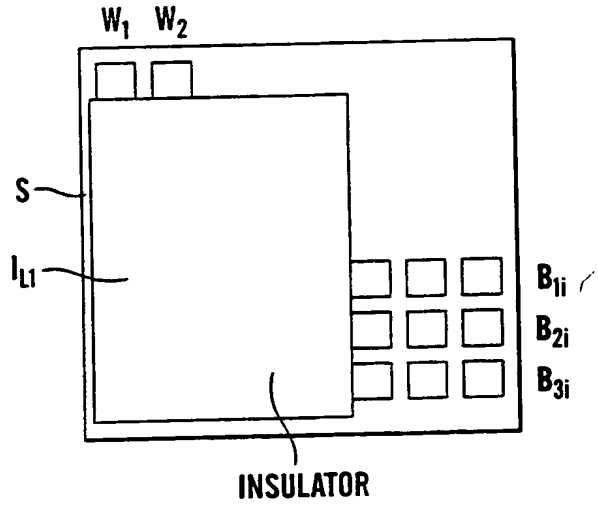


Fig.11b

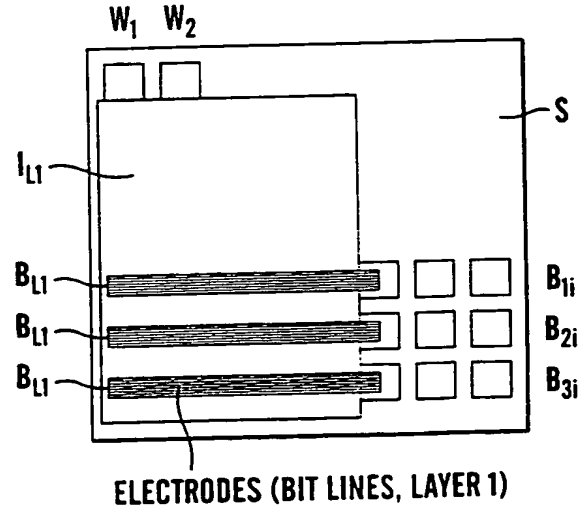


Fig.11c

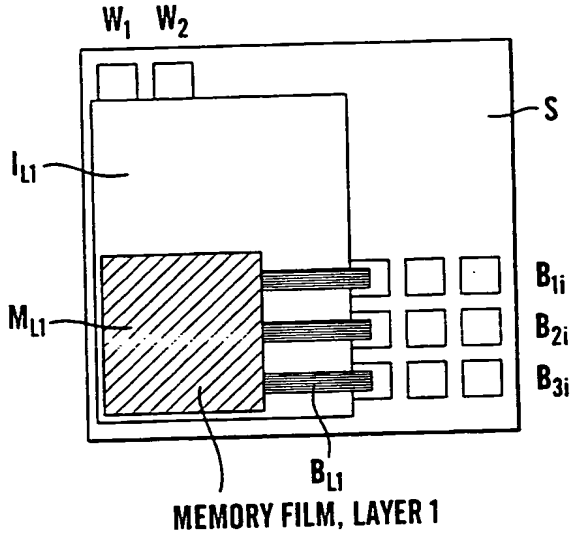


Fig.11d

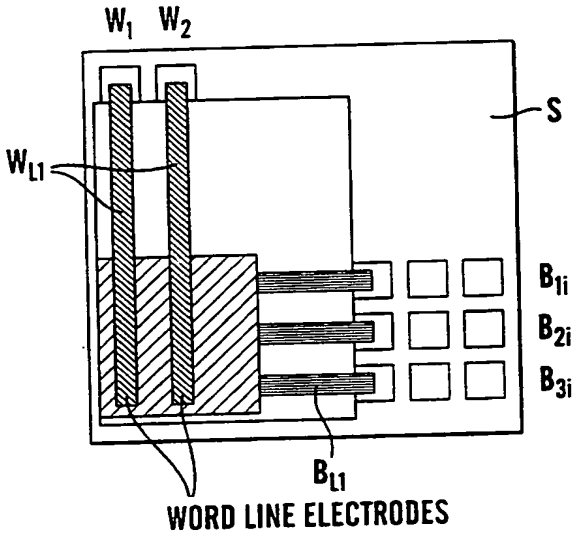


Fig.11e

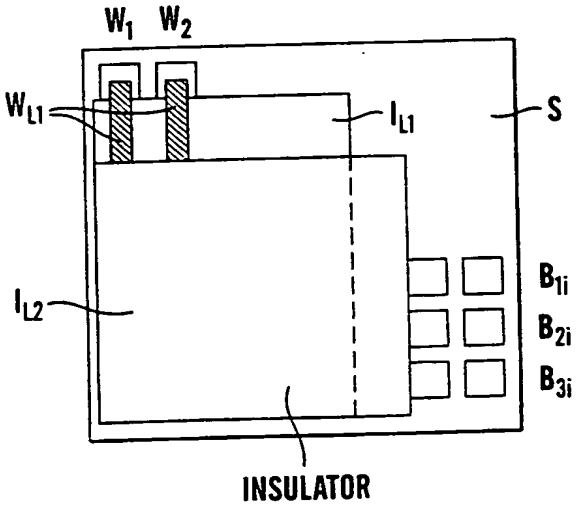


Fig.11f

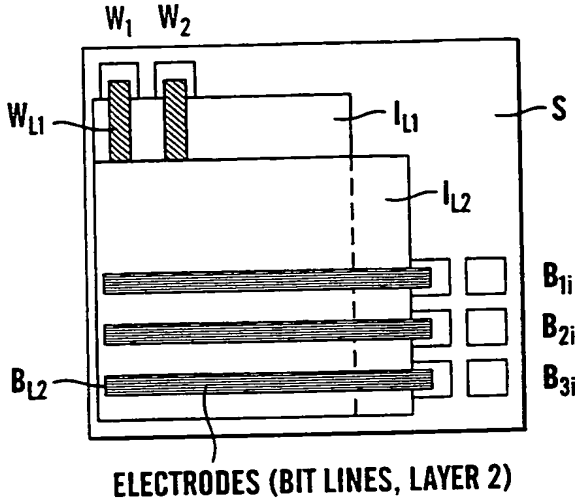


Fig.11g

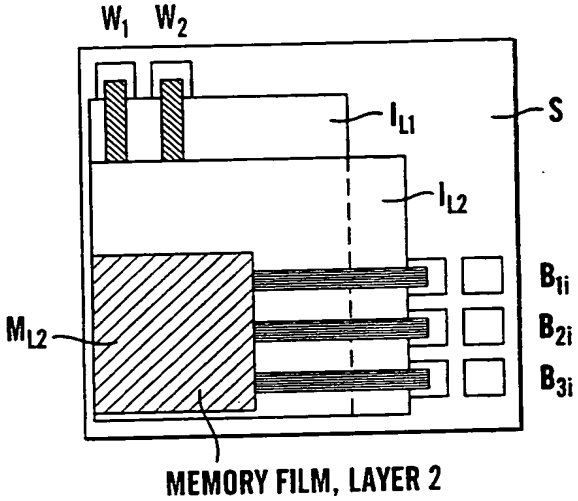


Fig.11h

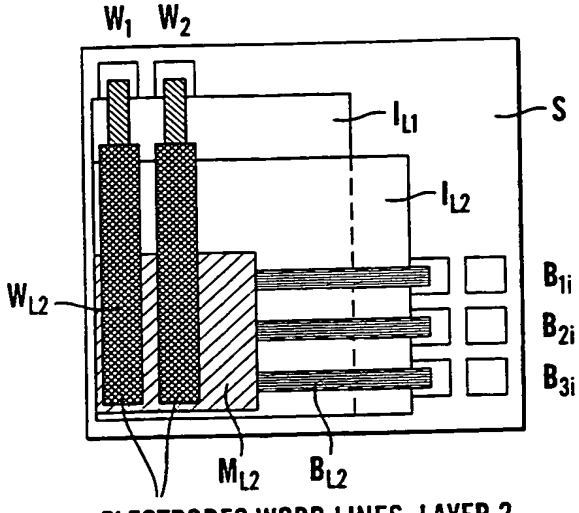


Fig.11i

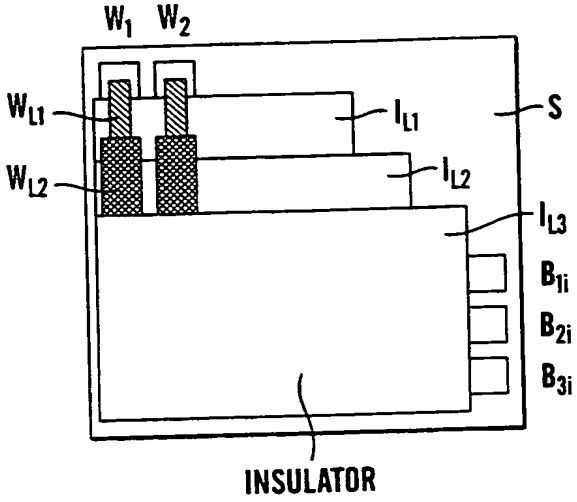


Fig.11j

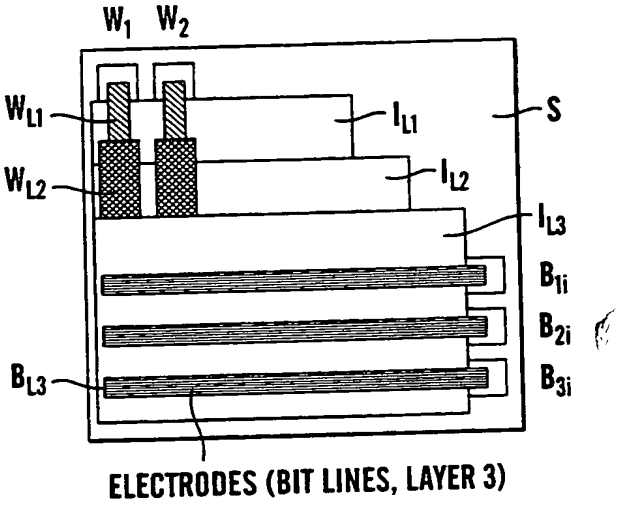


Fig.11k

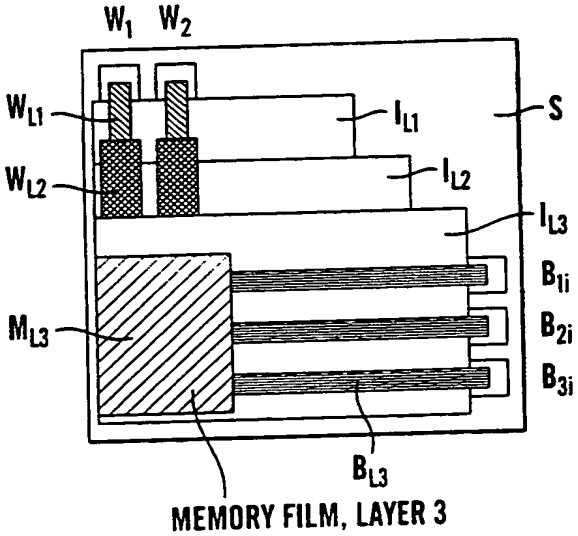


Fig.11l

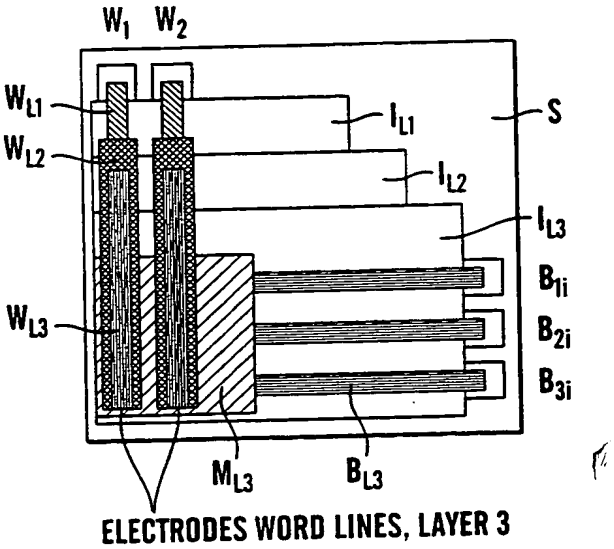

W1 W2
WL1
WL2
WL3
IL1
IL2
IL3
S
B1i
B2i
B3i
ML3
BL3
ELECTRODES WORD LINES, LAYER 3

Fig. 11m

09/926531

PCT/NO01/00113

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Commissioner
US Department of Commerce
United States Patent and Trademark
Office, PCT
2011 South Clark Place Room
CP2/5C24
Arlington, VA 22202
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in its capacity as elected Office

Date of mailing (day/month/year) 05 April 2002 (05.04.02)	
International application No. PCT/NO01/00113	**Applicant's or agent's file reference** Opti49PCT
International filing date (day/month/year) 15 March 2001 (15.03.01)	**Priority date** (day/month/year) 15 March 2000 (15.03.00)
Applicant NORDAL, Per-Erik et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

16 October 2001 (16.10.01)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No.: (41-22) 740.14.35

Authorized officer

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